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**INVESTIGATION OF ZnSe AND ZnS_xSe_{1-x}
FOR APPLICATION IN THIN FILM SOLAR CELLS**

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A thesis submitted in partial fulfilment
of the requirements of the
University of Northumbria at Newcastle
for the degree of
Doctor of Philosophy

Research undertaken in the School of Computing,
Engineering & Information Sciences

November 2005

To
Bev, my rock and best friend
and
Sam and Kelsey, two wonderful girls.

Abstract

Successful deposition of ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers has been performed with close-spaced thermal evaporation (CSTE). ZnSe ($E_g = 2.67\text{eV}$) and $\text{ZnS}_x\text{Se}_{1-x}$ (E_g to 3.6eV) have the potential to replace CdS ($E_g = 2.42\text{ eV}$) as a buffer layer in solar cell applications, giving a two-fold benefit: (i) increased blue response of the cell, potentially allowing more light to reach the pn junction and contribute to photogeneration and (ii) reduce the toxic Cd element of the buffer layer. CSTE has produced films in which the deposition parameters can be controlled to alter the morphology of the as-deposited coatings. SEM and AFM investigations have shown that pinhole free ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ films can be produced with this deposition process. In addition, the $\text{ZnS}_x\text{Se}_{1-x}$ layers show a linear shift in lattice constant and a systematic shift in energy bandgap with alloy composition. XRD data and the steep absorption edges in the transmittance data confirm the good crystallinity of the layers.

To partner the ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ buffer layers in a thin film heterojunction, CdTe absorber layers were grown in the superstrate configuration. These CdTe layers were deposited in the same deposition chamber, without breaking vacuum, to reduce the risk of interfacial contamination. ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe solar cells were fabricated with the best cell producing PV characteristics of: short circuit current 17mAcm^{-2} , open circuit voltage 460mV and efficiency approaching 3%. The spectral response of all ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe devices demonstrated a systematic shift to shorter wavelengths with increasing alloy composition, therefore showing the potential of these materials to increase solar cell efficiency. This low cost deposition process has shown excellent potential to be scaled up for commercial applications.

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Chapter One

Introduction

1.1 Introduction

Photovoltaic solar cells are used for supplying power for satellites, consumer products, e.g. calculators, and for supplying power for water pumping in remote locations. The most developed solar cells are made using crystalline silicon. This solar cell essentially consists of a p-type silicon wafer cut from a silicon boule which is grown using the Czochralski method, the surface of which has been compensation doped to form an n-type layer [1]. Efficiencies approaching 25% have been demonstrated for cells made in the laboratory and foot square modules have been produced with efficiencies $> 20\%$ [2]. The cost of producing the silicon wafers makes this type of solar cell expensive and prohibits the more extensive use of photovoltaics to generate power on a large scale. A less expensive approach for producing cells and modules is to make them using thin film technology [3]. This technology involves depositing thin films of n and p-type materials and a back contact material onto glass substrates using low cost deposition methods. The constructed cell is much thinner than its wafer counterpart, typically < 10 microns compared to 100's microns. It is also possible to produce larger solar cells, as large glass sheets are easier to manufacture than large semiconductor wafers.

Thin film devices can be made from many semiconductor materials, but in practice, only a few materials are stable enough to be of interest for making commercial devices and modules [4]. The most investigated materials are amorphous silicon, copper indium diselenide and cadmium telluride [5]. Historically it was thought that amorphous silicon devices would be the ideal thin film material and it has indeed had substantial success for small-scale applications, e.g. supplying power for calculators and for charging batteries. The efficiency of such devices however degrades under illumination due to the so-called Staebler-Wronski effect, with module efficiencies dropping to $< 5\%$ over time [6]. The advantage of the other thin film materials is that modules can be made with stable efficiencies in excess of 10%. Cadmium telluride (CdTe) has the best properties for photovoltaic applications in terms of energy bandgap and ease of deposition and small area cells with efficiencies $> 16\%$ have been reported [7]. As CIS (CuInSe_2) and CdTe are used as p-type absorber layers, an n-type buffer layer is required to produce a pn junction device. For CdTe technology, the most common structure is made by depositing a thin layer of n-

CdS onto SnO₂ coated glass, followed by the p-CdTe; a back contact material is then deposited to complete the device. A major problem with this technology is that cadmium is a toxic element and despite the fact that it is used in the form of compounds, there is concern regarding safety issues with respect to the manufacture, use and disposal of these modules. This has also taken on new impetus as the European Community has introduced the RoHS directive [8], which will restrict the use of cadmium in certain electrical goods from July 2006. The directive states that cadmium should not be more than 0.01% per homogeneous element, but at present Cd in solar cells is exempt. However, it may only be a matter of time before this exemption is removed. In Germany, they have minimised this problem by developing CuInSe₂ based cells [9]. The current buffer layer used however is CdS, although in the form of a very thin layer.

Current efforts to improve the thin film solar cells based on both absorber layers are to:

1. Use wider bandgap buffer layers to permit more light to reach the junction, consequently improving the blue response of the cells to improve the cell efficiencies.
2. To minimise / eliminate the concentrations of toxic elements used in manufacture, especially cadmium.
3. To improve the back contacts to improve cell stability.

The work reported here attempts to contribute to 1 and 2 above by the development of buffer layers based on the use of ZnS_xSe_{1-x}. ZnSe has a larger bandgap than CdS and should allow more light to pass without being absorbed. Incorporating S into the ZnSe to form ZnS_xSe_{1-x} will widen the energy bandgap further, although adding too much could result in the layers being too resistive for use in solar cell devices. Preliminary work by Bube indicates that the contact potential of the junction, formed between ZnS_xSe_{1-x} and CdTe, is amongst the highest out of the II-VI alloys / compounds available to make window layers and hence this combination has excellent potential [10].

It is the aim of this research to grow and characterise ZnS_xSe_{1-x} buffer layers for use with CdTe absorber layers. These layers will be deposited using a low cost physical deposition process and the structure and physical properties of these layers

determined and correlated to the deposition conditions. Optimised layers will then be used to produce n-ZnS_xSe_{1-x} / p-CdTe devices.

1.2 Material Aspects of Solar Cells

1.2.1 A Brief History

In 1839, Becquerel was first to demonstrate a photovoltaic effect whilst illuminating platinum electrodes (coated with AgBr or AgCl) placed in an acidic solution (electrolyte), [11]. Adams and Day [12] later showed a photoconductive effect from Pt inserted into solid selenium. The first pn junction solar cells were produced by slow solidification of molten silicon as described in 1941 by Ohl [13].

In parallel to silicon development of the 70's was the introduction of heterojunction devices. The use of III-V compounds and alloys and interest in thin film II-VI and I-III-VI₂ compounds have all led to significant progress in the efficiency of solar cells, which are again described in more detail later.

It should be noted that comparison between solar cell device performances is usually accomplished by quoting cell conversion efficiencies. A cell's production cost in tandem with its generation potential is in some quarters deemed more representative to consumer and industry needs. However, this debate is ongoing and possibly will be for some time yet [14]. Also, the discussions here will concentrate on research devices of single cells and not necessarily solar cell modules.

1.2.2 Crystalline Silicon Cells

In 1954, Chapin [15] of Bell Laboratories developed the first silicon solar cell with an efficiency of 6%. Much of the technology used in the development of early silicon cells was borrowed from the microelectronics industry. At this time transistors were in production, fabricated from high purity single crystal silicon, which turned out to be a good material for solar cell research. Silicon is extracted from quartz or even sand and refined to a high purity. The silicon wafers are grown using the Chochralski method. This procedure uses a melt, from which the single crystal silicon boule is drawn. The boule, or ingot, is then cut into thin wafers usually between 0.2 to 0.5 mm thick. This is a costly procedure as not only half of the wafer is lost during

cutting but also diamond-cutting tools are required due to the material properties of silicon. Before a solar cell device can be fabricated, the wafer must be etched not only to repair the damage caused during cutting but also to prepare it for junction formation. During the crystal growth an impurity was added to the melt to dope the silicon. The two most common doping materials are boron for p-type and phosphorus for n-type regions. Also, due to a longer minority carrier diffusion length, the p-type semiconductor is usually the absorber material. Therefore, if this p-type wafer is heated in the presence of, say phosphorus, an n-type layer can be formed on the surface. Finally the front and back contacts (often silver) are made to the junction to form the device and an insulating material deposited to the front of the cell to form an antireflection coating. The best laboratory efficiency for single crystal silicon cells is currently $> 24\%$ [2]. Disadvantages of crystalline silicon are low absorption coefficient, material costs due to the fabrication technique and the indirect bandgap of silicon. However, high efficiency and the abundance of quartz or sand are advantageous to silicon development. Also, the problem encountered with minority carrier diffusion length can be partly overcome by using optical confinement, in which a reflecting back coating is included in the design to increase the path length of the incident light.

1.2.3 Multicrystalline Silicon

The cost of producing the wafer is the major problem with crystalline silicon solar cells. To overcome this obstacle, block casting was developed. The melted silicon is poured into graphite cubes and controlled cooling produces multicrystalline silicon blocks. The quality of this material is lower than that produced using the Chochralski method and therefore cast wafers can only be used for solar cell (and not microelectronic) devices, albeit with lower efficiencies.

1.2.4 GaAs and InGaAs

GaAs solar cells were first demonstrated in the 1960's. Adding a AlGaAs window, thus forming a heterojunction, increased the efficiency and cell area of these devices still further [16]. GaAs layers are been grown by advanced growth methods

such as epitaxial growth (LPE or MBE). A polished bulk grown substrate (i.e. wafer) is used as a seed for the epitaxial growth, therefore the new crystal layer has the same or similar properties to the substrate wafer. Advantages of GaAs over Si are higher conversion efficiency, improved radiation resistance (for space use), a direct bandgap and better thermal and lattice matching across the junction. However, material costs are still high when compared with other solar cell materials.

1.2.5 Thin Film Cells

A way to overcome the problems associated with crystalline material costs is to use thin film coatings. Not only are the production methods more cost effective but also the amount of material used is significantly less. The thickness of a thin film cell is in the region of a few microns, whereas a silicon wafer is at least 100 microns thick. These layers are deposited by a number of different methods and have permitted the development of thin film heterojunction based solar cells. Many polycrystalline thin film materials have been investigated over the years, but the three main materials that are still of research and commercial interest are amorphous silicon, copper indium diselenide (and alloys) and cadmium telluride.

1.2.5.1 Amorphous Silicon

The first amorphous silicon solar cells were produced in 1976 [17]. Amorphous silicon is actually a Si-H alloy with hydrogen content of approximately 10 to 20%. The layers are deposited in a plasma at low temperatures by decomposing the gas silane (SiH_4). Due to the material properties of amorphous silicon, an ideal cell design is where the pn junction is stretched out as far as possible. To achieve this, an insulating material separates the doped n and p-type regions. The strength of the electric field across the insulating region is a function of its thickness and contributes to the device performance. Due to low deposition temperatures, amorphous silicon has found many applications in consumer products such as calculators.

1.2.5.2 Copper Indium Diselenide (CuInSe_2)

The first reported CuInSe_2 (CIS) cell dates back to 1974, where a CdS buffer was deposited onto single crystal CIS with a conversion efficiency of 12% [18]. Other cell configurations soon followed and the first thin film CdS/ CuInSe_2 device, with an

efficiency of 6.6%, was reported in 1976 [19]. The absorber layer can be fabricated using two different techniques, co-evaporation of the elements or the selenisation of the pre-deposited In and Cu precursors. Devices are usually produced in the substrate configuration, in which the back contact (e.g. molybdenum) is deposited onto glass, followed by the chalcopyrite, then the window and finally TCO (transparent conducting oxide). With the addition of other elements, CIS has now developed into a range of alloys which include Copper Indium Gallium Diselenide, CuInGaSe_2 (CIGS) or Copper Indium Disulphide (CuInS_2). Device efficiencies of over 18% [2] have been demonstrated with CdS buffer layers. An aspect of current CIS work is to replace the CdS layer with a material that is cadmium free, one prospective candidate being ZnSe [20]. CIS has a direct bandgap but has an energy bandgap of 1.05eV, which is considered low (see figure 1.1). However, these solar cells have produced the best performances from all the thin film solar cells.

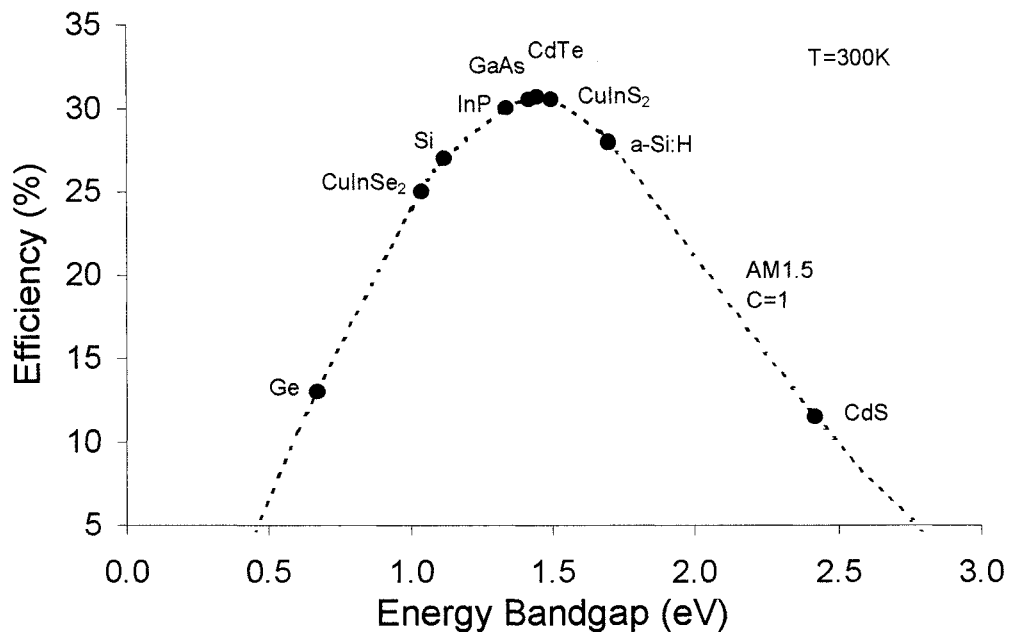


Figure 1.1. Graph of Efficiency as a function Energy Bandgap for Various Semiconductors [redrawn from 21].

1.2.5.3 Cadmium Telluride (CdTe)

Interest in the potential of CdTe dates back to 1956 in which the theoretical optimum efficiency as a function of energy bandgap for various absorbers was produced [22]. This showed that the ideal energy bandgap for a homojunction solar cell is approximately 1.5eV, see figure 1.1. Early devices developed by Cusano [23] using a Cu_2Te / CdTe structure proved to be unstable. The first thin film CdS / CdTe heterojunction solar cell was produced in 1969 [24] with an efficiency of only 1%. This however, proved to be the catalyst for research into CdS / CdTe heterojunctions with 6% efficiency cells emerging in 1972 [25] and almost 16% efficient cells in 1992 [26]. A more in-depth discussion of CdTe and its window partners will be introduced in chapter 3.

1.2.6 Dye-Sensitised Cells and Other Approaches

To overcome some of the material and cost implications of crystalline and thin film cells, other approaches to photovoltaic generation have been investigated. In a pn junction, the transport mechanism and light absorption occur throughout the device, however dye cells use a different approach [27]. A porous layer of titanium dioxide (TiO_2) nanocrystals is coated with a monomolecular layer of dye molecules and immersed in an electrolyte, see figure 1.2. In a process comparable to photosynthesis, the dye molecules absorb light and the excited electrons are transferred to the titanium dioxide conduction band. The electrolyte, TCO and external load complete the circuit. A novel aspect of dye cells is their ability to only absorb a band of photons rather than all photons with energies greater than the energy bandgap, as with conventional solar cells. This feature could lead to dye sensitised “window” modules that transmit light in the visible but absorb in the infrared.

Another approach is to stack several cells with different bandgaps on top of one another. With the energy gap decreasing from the illuminated surface, each cell converts only part of the spectrum and the total efficiency is the accumulation of all the devices. Concentrator cells on the other hand, use an optical arrangement to track the sun. If the concentration factor is high, then even the cost of crystalline materials can be deemed insignificant when compared to large-scale system cost.

More recently the HIT (heterojunction with intrinsic thin layer) cell has been developed [28], which combines crystalline and amorphous silicon in the same unit.

The n-type c-Si has an intrinsic layer of a-Si:H (hydrogenated a-Si) coated on either side. There then follows an n-type and p-type a-Si:H coating on each intrinsic layer to which the TCO and contacts are applied. Efficiencies of 21% have been reported with 10cm x 10cm cells and 18.4% for 80cm x 120cm modules.

Most of the discussion so far has been concerned mainly with the absorber material parameters, however the heterojunction window partner also plays an important role in the characteristics of photovoltaic conversion. The material interface and optical properties of these buffer layers are just as important to that of the absorber layer. Therefore this topic, in terms of CdTe absorbers, will be covered in more detail in chapter 3.

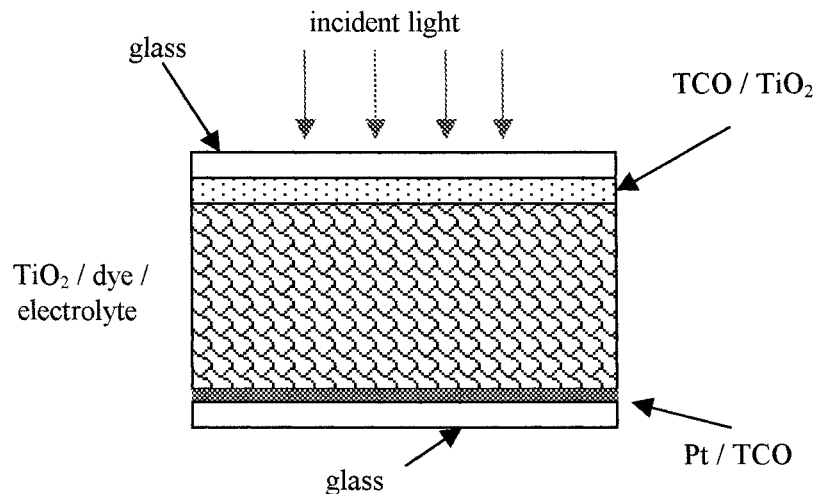


Figure 1.2. Cross Section of a Dye-Sensitised Solar Cell.

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Chapter Two

Solar Cell Concepts and Background Theory

The principle behind a solar cell device is the direct conversion of solar radiation into electricity. At the heart of most solar cells is a p-n junction, fabricated using two different structures. The homojunction is formed from the same semiconductor material, however compensatory doping is used to alter the conductivity type of part of the device, whereas a heterojunction is fabricated using two separate semiconductor materials. Solar cells depend on light being absorbed in the semiconductor p-n junction device. When incident photons with a greater energy than the energy gap of the p-type material are absorbed, electron-hole pairs are generated, thus raising electrons from the valence band to the conduction band. The internal electric field of the space charge region, formed by the p-n junction, separates the diffused excess minority carriers, whereupon they are pushed through to an external detection circuit generating a current, see figure 2.1. However, some of the electron-hole pairs created in the absorber layer do not diffuse to the junction. Losses are primarily due to bulk recombination in the absorber layer or recombination at the junction between the p and n-type semiconductors.

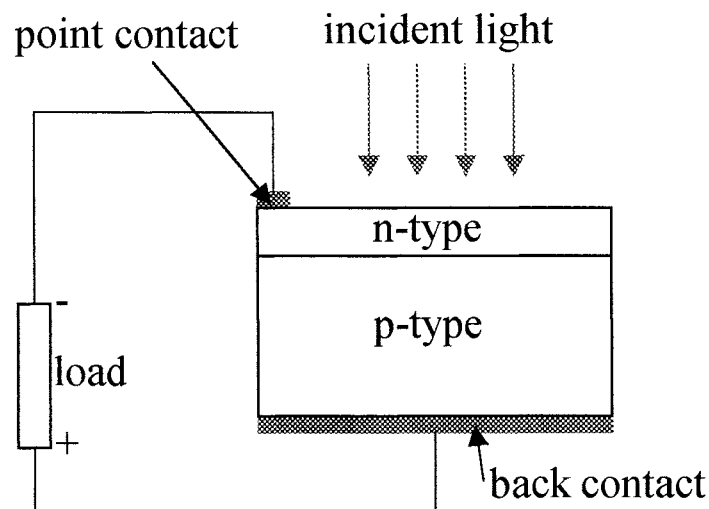


Figure 2.1. Schematic Diagram of a Solar Cell.

A requirement for efficient solar cells is that the minority carrier diffusion length (the distance carriers travel before recombination) is much greater than the absorption length, L_{α} (the thickness of the material required to absorb $1/e$ of the

incident photons). The p-type material is generally used as the absorber layer because the minority carrier diffusion length is longer in p-type semiconductors (i.e. electrons) than in n-type (i.e. holes). The n-type layer in this case is known as the window layer. Unique to heterojunctions is the ability to choose a material with a large energy band gap that will allow, in principle, more light to reach the p-n junction.

2.1 Solar Radiation

Critical to all photovoltaic systems is the energy they receive from the sun. The sun itself can be approximated to a black body with a temperature of 5800K and with 98% of its total energy, in outer space, lying between the wavelengths of 0.25 and 3.0 μm . An important quantity associated with this is the solar constant, defined as the rate at which energy is received on the earth at an average distance from the sun with an accepted value is 1353 Wm^{-2} [1]. Unfortunately the earth's atmosphere attenuates much of this radiation, the main causes of this being scattering by molecules and dust particles, figure 2.2 [2].

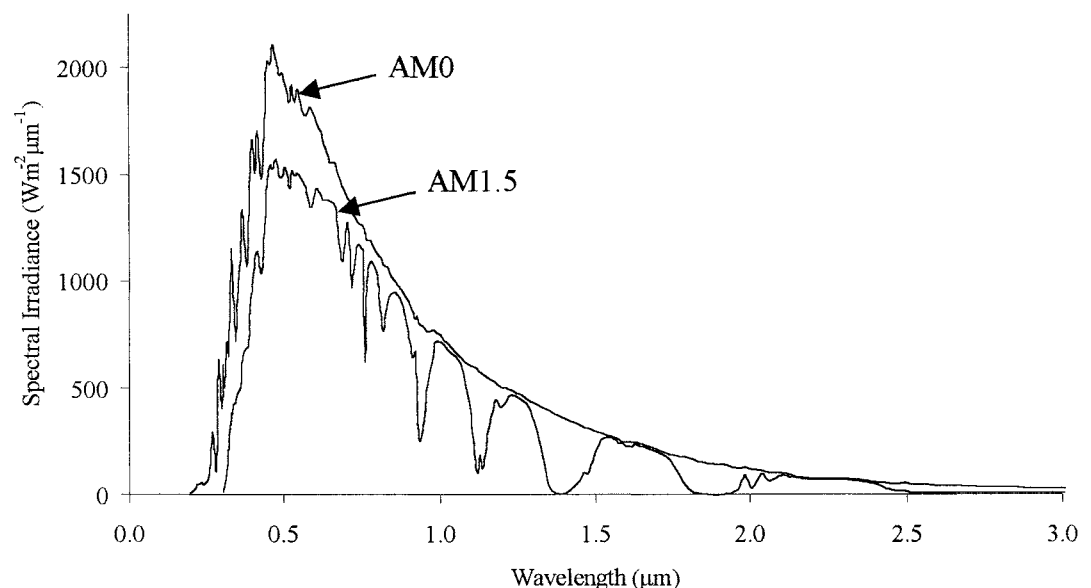


Figure 2.2 Solar Spectrum Irradiance Curves as a Function of Wavelength [3].

To take attenuation into consideration when using a simulator to test solar cell parameters, a standardised system has been introduced. The most important

consideration is the angle through the atmosphere that the sun's energy can potentially take, thus described by the relative air mass (AM) number. Solar radiation on the surface of the earth's outer atmosphere is described as being AM0. If the atmosphere is given a value of unity, then on the earth with the sun directly overhead, the air mass value will be AM1. However, when the sun is at an angle θ the air mass is given by $AM(\sec \theta)$ as shown in figure 2.3.

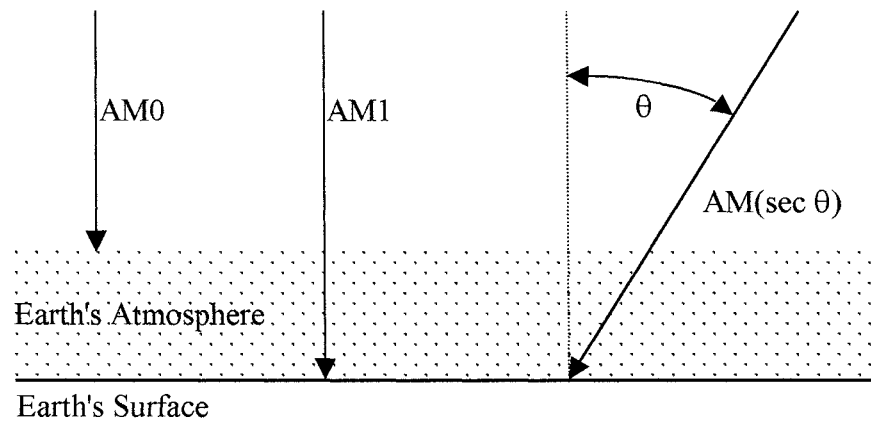


Figure 2.3. Solar Radiation Spectrum [1].

The air mass number only describes the spectral content of the radiation and does not disclose its intensity. It is therefore necessary to describe illumination in terms of power per unit area. For AM0 this is the solar constant and for AM1.5 1000 Wm^{-2} [1].

2.2 The Homojunction

The homojunction is a p-n device manufactured from the same semiconductor material, e.g. a junction with a single energy bandgap. The ideal abrupt homojunction is essentially the ideal p-n junction. In this ideal case the semiconductor is assumed to be perfect crystal and there is a step change in doping from the p to n-type sides.

2.2.1 The p-n Junction Diode

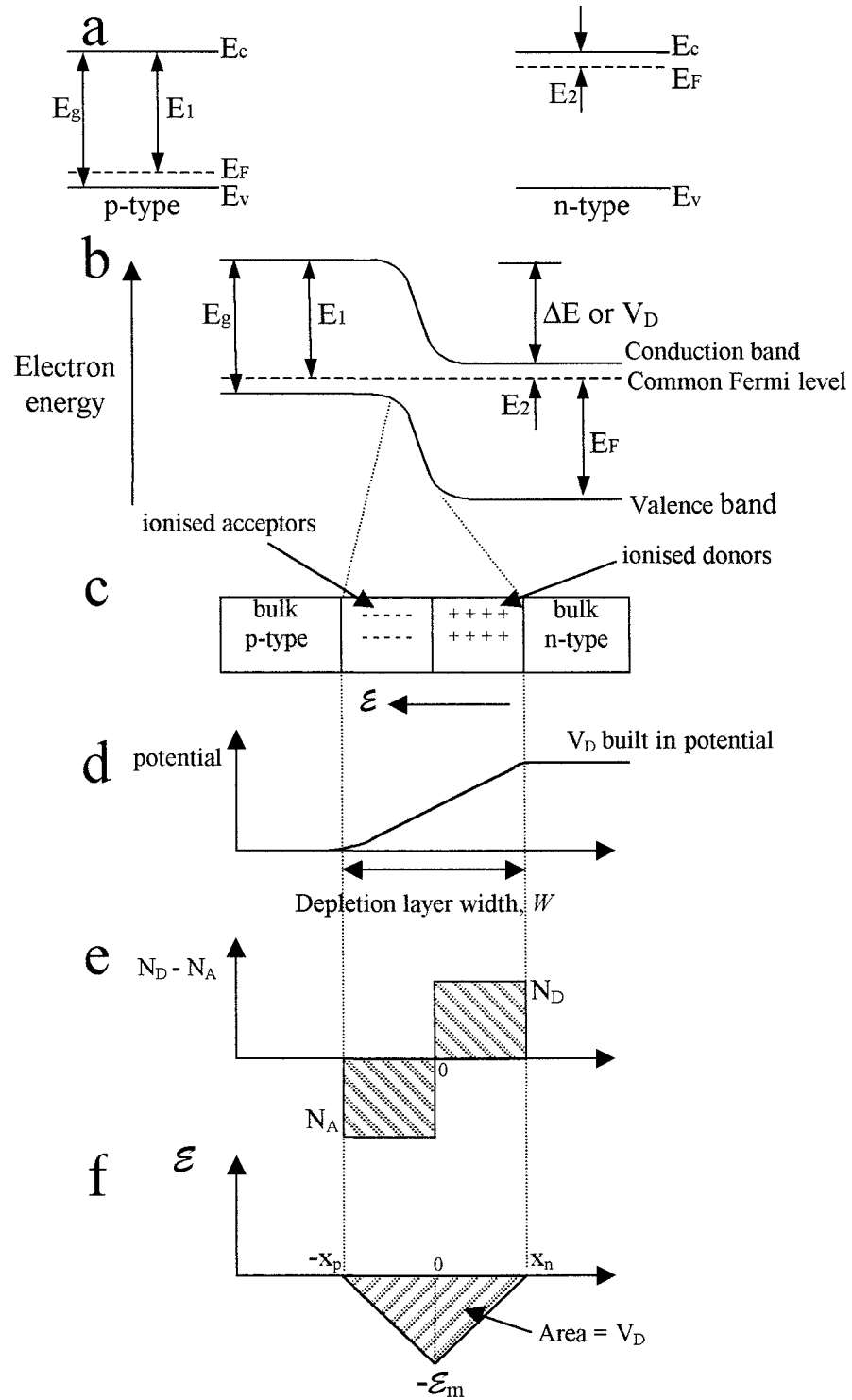


Figure 2.4. (a) Isolated p-type and n-type Materials; (b) Formation of a pn Junction; (c) The Space Charge Region; (d) Potential Difference Distribution; (e) Rectangular Approximation of the Space Charge Distribution; (f) Electric Field Distribution [4].

The operation of a pn junction can be explained by examining the interaction between two isolated p-type and n-type semiconductor materials brought together to form an abrupt junction, as shown in figure 2.4 [4]. Upon first making contact, electrons diffuse from the n-region to the p-region due to the concentration gradient that has formed. The diffusion of these electrons form a positively charged depletion layer of ionised donors close to the metallurgical junction. Similarly, holes diffuse from the p-region to the n-region and a corresponding negatively charged depletion layer of ionised acceptors form in the region near to the junction. The two regions together form the depletion layer or space charge region, which has an electric field directed from the positive to negative sides of the depletion layer. The diffused carriers that cross the junction become minority carriers, the excess of which form a minority carrier concentration gradient. The charge separation and its electric field effectively become too large and prevent further diffusion and so equilibrium is reached. At equilibrium, the net current flow (electron and hole drift or diffusion) across the junction is zero. The Fermi levels are aligned across the junction, however, as the Fermi levels in the bulk n and p-regions are fixed due to the band structure, this is achieved by p-region rising relative to the n-region. Also at equilibrium, an electrostatic potential is established across the junction which is called the contact, diffusion or built in potential and is related to the impurity concentrations by [4]

$$V_D = \frac{kT}{e} \ln \frac{N_A N_D}{n_i^2} \quad 2.1.$$

where N_A and N_D are the acceptor and donor impurity densities respectively and n_i^2 is the intrinsic carrier density. The total stationary charge of the space charge region is zero, therefore the widths of the two depletion regions depend upon the original doping level of the n and p-regions. To maintain the overall space charge neutrality, the total positive space charge per unit area on the n-side of the junction must equal the total negative space charge per unit area on the p-side:

$$N_A x_p = N_D x_n \quad 2.2.$$

Therefore, the depletion width, W , is given by

$$W = x_p + x_n \quad 2.3.$$

Integration of Poisson's equations (for abrupt junction approximation) gives the electric fields [5]:

$$\mathcal{E}(x) = -\frac{eN_A(x+x_p)}{\epsilon_s} \text{ for } -x_p \leq x < 0 \quad 2.4.$$

and

$$\mathcal{E}(x) = -\mathcal{E}_m + \frac{eN_D x}{\epsilon_s} \quad 2.5.$$

$$\mathcal{E}(x) = \frac{eN_D(x-x_n)}{\epsilon_s} \text{ for } 0 < x \leq x_n \quad 2.6.$$

The maximum electric field \mathcal{E}_m that exists at $x = 0$ is given by [5]

$$|\mathcal{E}_m| = \frac{eN_D x_n}{\epsilon_s} = \frac{eN_A x_p}{\epsilon_s} \quad 2.7.$$

The potential distribution, $V(x)$, can now be found by a second integration of Poisson's equations:

$$V(x) = \mathcal{E}_m \left(x - \frac{x^2}{2W} \right) \quad 2.8.$$

And the built in potential:

$$V_D = \frac{1}{2} \mathcal{E}_m W \equiv \frac{1}{2} \mathcal{E}_m (x_n + x_p) \quad 2.9.$$

By eliminating \mathcal{E}_m from equations 2.7 and 2.9 we find the depletion width for a two-sided abrupt junction [5]:

$$W = \sqrt{\frac{2\epsilon_s}{e} \left(\frac{N_A + N_D}{N_A N_D} \right) V_D} \quad 2.10.$$

In the case where one side of the junction is more heavily doped than the other side, a one sided abrupt junction is formed. If, say the n-region is more heavily doped than the p-region (i.e. $N_D \gg N_A$), then according to equation 2.2, the depletion layer width on the n-side is much smaller than the p-side ($x_p \gg x_n$) and equation 2.10 reduces to

$$W \approx x_p = \sqrt{\frac{2\epsilon_s V_D}{eN_A}} \quad 2.11.$$

For the above case the one-sided abrupt junction, corresponding space charge region and electric field distribution are shown in figure 2.5 [5].

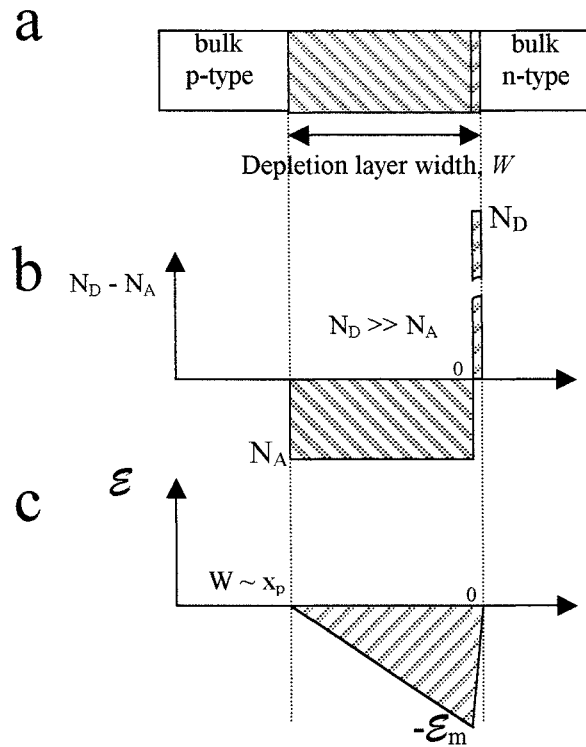


Figure 2.5. One-Sided Abrupt Junction, With $N_D \gg N_A$; (a) The Junction Depletion Region; (b) The Space Charge Distribution; (c) Electric Field Distribution [5].

The two space charge regions forming the depletion layer of the pn junction have a capacitive component when placed under a bias voltage. The width of the depletion region, and hence its capacitive charge, vary with reverse bias voltage.

Junction or depletion layer capacitance can be modelled by that of a parallel plate capacitance, thus defined by [1]

$$C = \frac{\epsilon_s A}{W} \quad 2.12.$$

where ϵ_s is the permittivity of the semiconductor, W the depletion width and A is the cross sectional area of the junction. Equation 2.10 shows the depletion width is related to the built in voltage and doping concentrations, therefore the capacitance for an abrupt junction per unit area can be written as [1]

$$C_J = \sqrt{\frac{e\epsilon_s}{2} \left(\frac{N_A N_D}{N_A + N_D} \right) \left(\frac{1}{V_D} \right)} \quad 2.13.$$

If however, the assumption is made that the n region is more highly doped than the p region (i.e. $N_D \gg N_A$), or the depletion region extends solely into the p-type layer, then equation 2.13 simplifies to the one sided abrupt junction

$$C_J = \sqrt{\frac{e\epsilon_s N_A}{2} \left(\frac{1}{V_D} \right)} \quad 2.14.$$

2.2.2 The p-n Junction and Applied Bias

In the case with no applied bias, and without illumination, the pn junction is in equilibrium. That is the net current flow of the four current components, electron and hole drift or diffusion, is zero, see figure 2.6. A few electrons in the conduction band of the n-type material have enough energy to overcome the potential barrier, V_D , and form a diffusion current flowing to the p-side (conventionally p-side to n-side). Also there is an electron drift current from the p-side to the n-side (conventionally n-side to p-side), which is opposite and equal in magnitude to the electron diffusion current. Similarly for holes, the diffusion current from the p- to n-side is opposite and equal to the hole drift current from the n- to p-side.

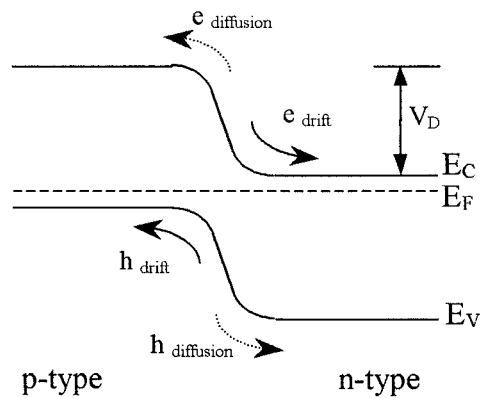


Figure 2.6. The Current Components of a pn Junction at Equilibrium.

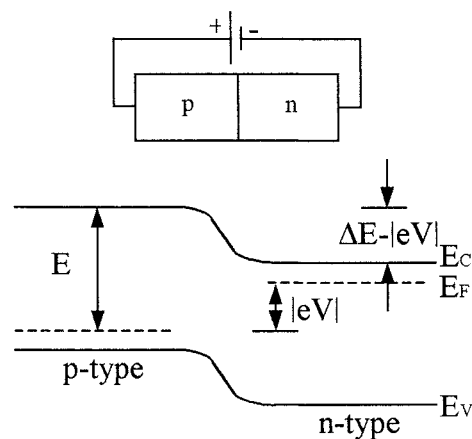


Figure 2.7. A Forward Biased pn Junction.

The stability described above can be altered by the introduction of an external applied bias. The case where the n-type material is connected to a negative potential and the p-type to a positive potential is known as forward biasing, see figure 2.7. The potential V decreases the energy difference between the two regions and in doing so, makes it easier for electrons in the n-side to diffuse to the p-side. Similarly, holes find it easier to diffuse from the p- to n-region. The overall effect is to increase the

diffusion currents by the Maxwell-Boltzmann factor $e^{\Delta E/kT} = e^{eV/kT}$. This alteration to the band structure has little effect on the drift currents, so the net electron current is

$$I_{ntot} = I_{ndiffusion} - I_{ndrift} \quad 2.15.$$

$$I_{ntot} = I_{ndrift} \exp^{eV/kT} - I_{ndrift} \quad 2.16.$$

$$I_{ntot} = I_{ndrift} (\exp^{eV/kT} - 1) \quad 2.17.$$

A similar expression can be found for the net hole current, and therefore the total current is [4]

$$I = I_{ntot} + I_{ptot} \quad 2.18.$$

$$I = I_o (\exp^{eV/kT} - 1) \quad 2.19.$$

where $I_o = I_n + I_p$ is called the reverse saturation current and is a constant characteristic of the junction. Equation 2.19 is often called the rectifier or Shockley equation and can also be written in terms of current density (current flowing per unit cross sectional area)

$$J = J_o (\exp^{eV/kT} - 1) \quad 2.20.$$

For the reverse bias configuration, the n-type material is connected to a positive potential and the p-type to a negative potential, see figure 2.8. Since the resistance of the depletion region is larger than that of the bulk, the diffusion voltage and external bias effectively appear across the depletion region only. The bias voltage increases the energy levels in the p-region and in doing so, increases the electron energy. Therefore, the potential barrier height is increased by the product of the electron energy and applied bias, $|eV|$. This increase in barrier height restricts the flow of the electron diffusion current from the n- to p-side, however, the electron drift remains almost unchanged. A similar effect is found with the holes and therefore the diffusion currents for both electrons and holes become very small. The process of explaining the currents can be obtained in a similar manner to that of the forward bias junction and it can be shown that equation 2.20 is valid for both positive and negative voltages.

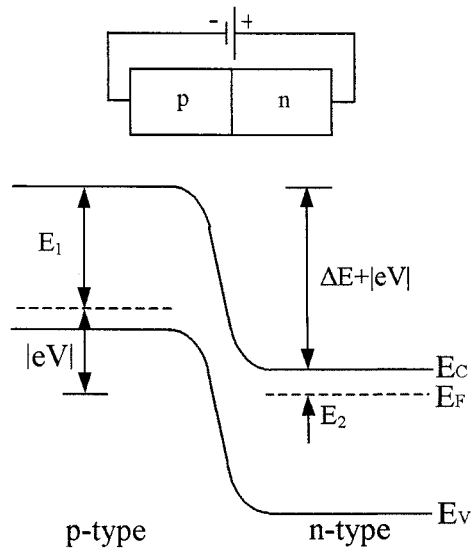


Figure 2.8. A Reversed Biased pn Junction.

A plot of a typical pn junction under forward and reverse bias conditions is shown in figure 2.9. When the potential is positive, the exponential term dominates and the diffusion current rises accordingly. However, under a reverse potential bias the diffusion current is reduced as fewer electrons can surmount the larger potential barrier.

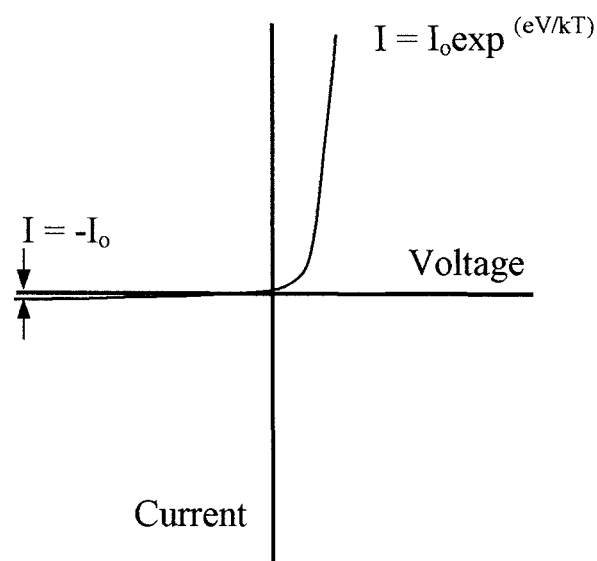


Figure 2.9. Typical Current-Voltage Characteristics of an Ideal pn Junction

2.2.3 Dark Current Characteristics of the Homojunction

When a forward biased solar cell is supplying power, a dark current exists that opposes the photocurrent. Therefore, determining the dark current-voltage characteristics of a solar cell is as important as determining the cell's illuminated behaviour. These current transport characteristics are covered in more detail by (Hovel ch 3 [6], Mitchell ch 2 [7] and Sze ch 2 [5]). There are three main transport mechanisms in a forward biased pn junction, the sum of which gives the total current flow across the junction: (1) injection (or diffusion) of carriers beyond the junction barrier, (2) recombination within the depletion region (3) multi-step tunnelling via defect energy states and recombination, all of which are represented in the energy band diagram of figure 2.10.

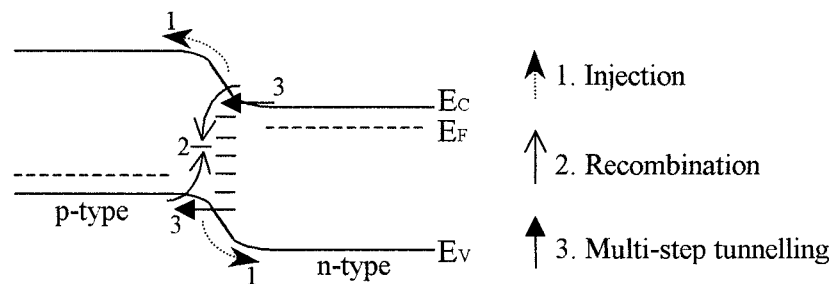


Figure 2.10. Current Transport Mechanisms in a Forward Biased p-n Homojunction; (1) Injection (2) Recombination within the Depletion Region (3) Multi-Step Tunnelling (and recombination) via Defect Energy States [7].

2.2.3.1 Injected Currents

When the doping levels on either side of the depletion region are constant, the electric field outside of the depletion region is virtually non-existent. In this case, the injection current can be approximated by the Shockley diffusion model as long as the following assumptions are made: (i) an abrupt depletion layer is required for the junction profile, (ii) Boltzmann Statistics apply to the model, (iii) the majority carrier densities are much larger than the injected minority carrier densities, (iv) no

generation or recombination is present in the depletion region, (v) depletion layer electron and hole currents are constant, (vi) the junction does not suffer from surface recombination effects. If these conditions are satisfied then the diode current density is given by [7]

$$J = J_o (\exp^{eV/kT} - 1) \quad 2.21.$$

where

$$J_o = e \left(\frac{n_p D_n}{L_n} + \frac{p_n D_p}{L_p} \right) \quad 2.22.$$

V is the junction voltage, n_p is the electron concentration in the p-side, p_n is the hole concentration in the n-side, D_n and L_n are the minority carrier diffusion coefficient and diffusion length in the n-type material, D_p and L_p are the minority carrier diffusion coefficient and diffusion length in the p-type material. The minority carrier concentrations at equilibrium are given by

$$n_p = \frac{n_i^2}{p_p} = \frac{n_i^2}{N_A} \quad 2.23.$$

$$p_n = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D} \quad 2.24.$$

where

$$n_i^2 = N_C N_V \exp^{-E_g/kT} \quad 2.25.$$

p_p and n_n are the hole and electron concentrations in the p- and n-type materials respectively, N_C is the effective density of states in the conduction band, whereas N_V is the effective density of states in the valence band. The Einstein relation for diffusion [8], $D = (kT/e)\mu$, can then be substituted to give the reverse saturation in terms of mobility [7]

$$J_o = kT n_i^2 \left(\frac{\mu_n}{N_A L_n} + \frac{\mu_p}{N_D L_p} \right) \quad 2.26.$$

2.2.3.2 Recombination within the Depletion Region

With the pn junction in forward bias, electrons and holes are injected across the junction. However, some of these carriers add to the dark current by recombining in the depletion region, forming a space charge layer recombination current (2 in figure 2.10). The assumptions made in the Sah-Noyce-Shockley [7] model are: (i) similar doping each side of the junction (ii) one recombination centre at the intrinsic Fermi level (iii) constant recombination rate in the depletion region. Therefore, under forward bias, the dark space charge recombination current density is [7]

$$J = \frac{en_i W}{\sqrt{\tau_{p0}\tau_{n0}}} \frac{2 \sinh\left(\frac{eV}{2kT}\right)}{e(V_D - V)/kT} f(b) \quad 2.27.$$

where n_i is the intrinsic carrier concentration, W the depletion layer width, V the junction voltage, τ_{p0} and τ_{n0} are the minority carrier lifetimes for the holes and electrons respectively and V_D is the diffusion voltage. The expression $f(b)$ is given by

$$f(b) = \int_0^\infty \frac{dx}{x^2 + 2bx + 1} \quad 2.28.$$

and

$$b = \exp^{-eV/2kT} \cosh\left[\left(\frac{E_t - E_i}{kT}\right) + \frac{1}{2} \ln\left(\frac{\tau_{p0}}{\tau_{n0}}\right)\right] \quad 2.29.$$

where E_t is the trap level and E_i is the intrinsic Fermi level.

Simplification of the term 2.27 can be achieved by substituting equation 2.25 and altering the conditions so that the n-side is more heavily doped than the p-side (i.e. $N_D \gg N_A$). Therefore the depletion width can be stated as

$$W = \sqrt{\frac{2\epsilon_s(V_D - V)}{eN_A}} \quad 2.30.$$

Also if the applied voltage is larger than $2kT/e$, $\sinh(eV/2kT)$ can be simplified to $\exp(eV/2kT)/2$ and the recombination current density can then be rewritten as

$$J = J_o(\exp^{eV/2kT}) \quad 2.31.$$

where

$$J_o = J_{oo}(\exp^{-E_g/2kT}) \quad 2.32.$$

and where [7]

$$J_{oo} = kT \sqrt{\frac{2N_c N_v \epsilon_s (V_D - V)}{e N_A \tau_{po} \tau_{no}}} f(b) \quad 2.33.$$

where ϵ_s is the semiconductor permittivity.

2.2.3.3 Multi-Step Tunnelling via Defect Energy States

The tunnelling current is caused by electrons tunnelling from the conduction band (and therefore holes from the valence band) to energy states within the forbidden region. This current can then either tunnel across the remainder of the junction or flow by a combination of tunnelling and recombination, illustrated as current 3 in figure 2.10. The tunnelling current density through states in the forbidden region for a pn junction is given by [7]

$$J = BN_t \exp\left(-\frac{4\sqrt{2m^*} E_B^{3/2}}{3e\mathcal{E}\hbar}\right) \quad 2.34.$$

and

$$\begin{aligned} E_B &\approx E_g - \delta_n - \delta_p - eV \\ E_B &\approx e(V_D - V) \end{aligned} \quad 2.35.$$

where B is a constant, N_t is the density of states available for tunnelling, m^* is the effective mass, E_B is the tunnelling energy barrier, \mathcal{E} is the electric field, δ_n is the displacement of the Fermi level from the conduction band in the n-region, δ_p the Fermi level-valence band displacement in the p-region and V is the applied voltage. The maximum electric field for an abrupt junction is given by

$$\mathcal{E} = \frac{2(V_D - V)}{W} \quad 2.36.$$

where the depletion layer under an applied bias is given by

$$W = \sqrt{\frac{2\epsilon_s}{e} \left(\frac{N_A + N_D}{N_A N_D} \right) (V_D - V)} \quad 2.37.$$

Substitution of equations 2.35, 2.36 and 2.37 into equation 2.34 gives [7]

$$J = J_0 \exp(\alpha V) \quad 2.38.$$

where

$$J_0 = BN_T \exp(-\alpha V_D) \quad 2.39.$$

and where

$$\alpha = \frac{4}{3\hbar} \sqrt{m^* \epsilon_s \left(\frac{N_A + N_D}{N_A N_D} \right)} \quad 2.40.$$

2.2.3.4 Collective Dark Current

The total dark current component is the sum of the injection, recombination and tunnelling currents. The main differences between the injection and recombination currents are their voltage, temperature and bandgap characteristics. According to equation 2.21 the injection current varies exponentially as $\exp^{(eV/kT)}$, whereas equation 2.31 shows that the recombination current varies with $\exp^{(eV/2kT)}$. Therefore the injected current will dominate with high forward biases while space charge recombination current will tend to dominate at low biases. The bandgap dependence with the injection current varies with $\exp^{(-E_g/kT)}$ and the recombination current with $\exp^{(-E_g/2kT)}$. This indicates that the space charge recombination current is more important at low temperatures and with larger bandgap materials.

2.2.4 The Homojunction under Illumination

When a homojunction is illuminated with photons of a greater energy than the bandgap of the junction material, electrons are excited from the valance to the conduction band leaving an equal number of holes. If this process takes place in the depletion region, then electrons drift to the n-type and holes to the p-type material due

to the existing electric field. In addition, if the electron-hole generation takes place within a distance smaller than the minority carrier diffusion length from the depletion region, these carriers will also contribute to the overall current flow. In order to calculate the potential volume of the junction to which generated carriers will contribute to the photocurrent, we can add the two minority carrier diffusion lengths of the p and n-type materials to the depletion region width and multiply by the product of the cross sectional area, as shown in diagram 2.11 and equation 2.41.

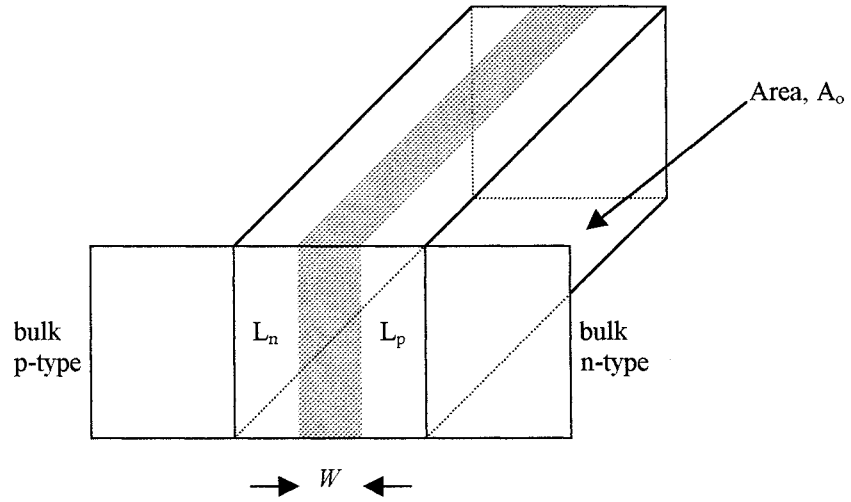


Figure 2.11 Diagram of the Photocarrier Generation Volume of the p-n Junction

$$Vol = (L_n + L_p + W)A_o \quad 2.41.$$

where L_n is the minority carrier diffusion length of electrons in the p-type material, L_p is the minority carrier diffusion length of holes in the n-type material, W is the depletion region width and A_o the cross sectional area of the device. Assuming that generation is uniform throughout this device volume then the photocurrent can be given by [8]

$$I_L = eGA_o(L_n + L_p + W) \quad 2.42.$$

where I_L is the light generated photocurrent and G is the number of electron-hole pairs generated per second, also known as the carrier generation rate. The ability of a

semiconductor to absorb photons is given by the absorption coefficient, α , of the material. The absorption coefficient not only depends upon the density of states in the conduction and valence bands but also the type of electron transition. For direct bandgap semiconductors such as CdTe, a transition from the valance to the conduction band only requires photon energy greater than the energy bandgap, $h\nu \geq E_g$. For indirect semiconductors such as Si, the electron still requires energy greater than the energy of the forbidden region, however because the highest energy point of the valance band does not coincide with the lowest point of the conduction band, a change in momentum is required. Consequently, direct bandgap materials have a steep absorption edge that allows the photons to be absorbed within a short distance of the material surface, whereas indirect bandgap materials require longer distances for absorption. A measure of this is the reciprocal of the absorption coefficient, the absorption length, L_α . Therefore to fabricate an efficient solar cell, the minority carrier diffusion lengths and the depletion width combined, $L_n + L_p + W$, need to be larger than the absorption length of the material, which for CdTe is approximately one micron and for silicon is tens of microns.

As previously discussed in section 2.2.3, the dark current takes the form

$$I = I_o (\exp^{eV/AkT} - 1) \quad 2.43.$$

where A is the ideality factor and can indicate the forward biased current mechanism of the solar cell. Under illumination, the photo-generated current is opposite in direction to the dark current and therefore equation 2.43 becomes [8]

$$I = I_o (\exp^{eV/AkT} - 1) - I_L \quad 2.44.$$

In this ideal case, the addition of photocurrent will have the effect of moving the dark current-voltage curve downwards by the magnitude of the photocurrent, as can be seen in figure 2.12.

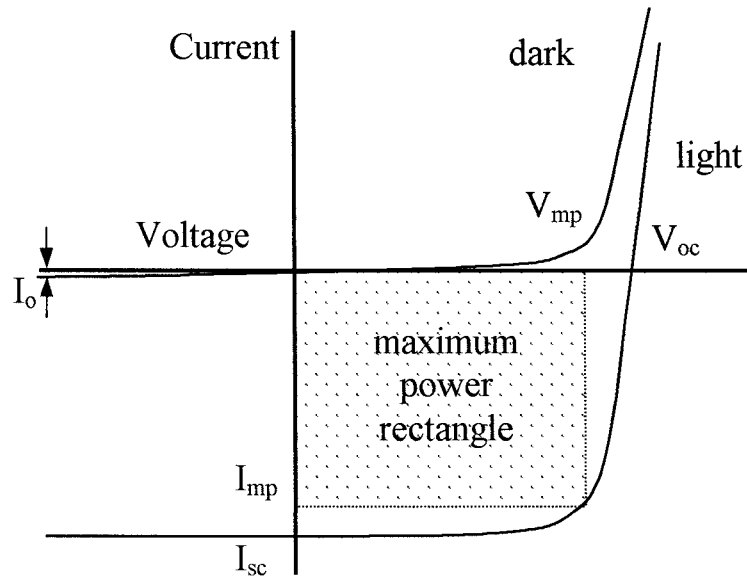


Figure 2.12. Typical Current-Voltage Characteristics of a pn Junction in the Dark and Under Illumination

The ideal solar cell can be represented by an equivalent circuit diagram, shown in figure 2.13. This places the photocurrent in parallel with the diode (p-n junction) and the total current, I , through the load resistance.

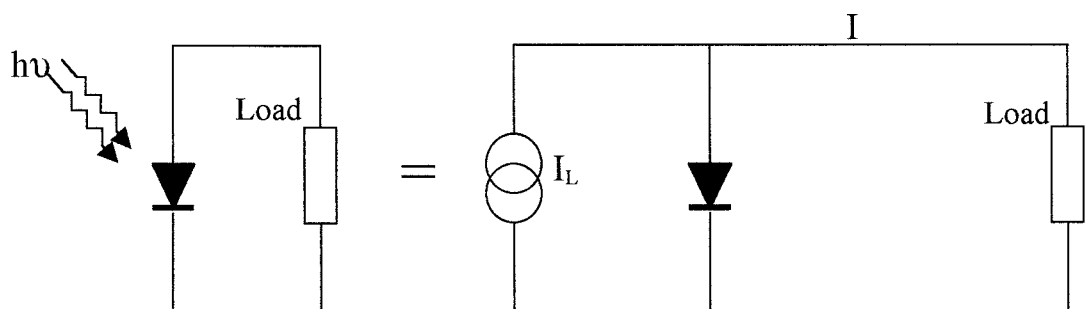


Figure 2.13. Equivalent Circuit of an Ideal pn Junction

A maximum current is obtained under short circuit conditions, that is when no output voltage is present and the load resistance is zero. For this ideal case, the magnitude of the photocurrent is equal to the short circuit current, I_{sc} , and therefore once again assuming uniform photocarrier generation

$$I_{sc} = |I_L| = eGA_o(L_n + L_p + W) \quad 2.45.$$

At the point where the current is zero, the maximum voltage is obtained. This is known as the open circuit voltage, V_{OC} , and is when the load resistance is infinite. Again for an ideal solar cell the open circuit voltage is given by [8]

$$V_{oc} = \frac{AkT}{e} \ln\left(\frac{I_L}{I_o} + 1\right) \quad 2.46.$$

and when $I_L \gg I_o$

$$V_{oc} \approx \frac{AkT}{e} \ln\left(\frac{I_L}{I_o}\right) \quad 2.47.$$

To obtain maximum power, the ideal solar cell cannot be operated in either short or open circuit conditions and the current-voltage product must be at a maximum, which is given by

$$P_m = I_{mp}V_{mp} \quad 2.48.$$

Maximum power is found when I_{mp} and V_{mp} are as close to I_{sc} and V_{OC} as possible, the ratio of which is given by the fill factor, FF, and is indicated on figure 2.12 as the maximum power rectangle [8]

$$FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}} \quad 2.49.$$

The efficiency of solar conversion, η , is arguably the most important photovoltaic property and is generally the first value that is used to compare solar cell behaviour. Solar cell efficiency is defined as the ratio of the power generated by the cell to the power of the incident light [8]

$$\eta = \frac{I_{mp}V_{mp}}{P_{in}} = \frac{I_{sc}V_{oc}FF}{P_{in}} \quad 2.50.$$

The equivalent circuit diagram of an ideal pn junction does not take into consideration resistances of the device. The resistance of the contacts and the bulk of the n and p-type materials contribute to the device series resistance, R_s . Ideally the series resistance should be zero but in practice R_s is typically less a few Ohms. High series resistance is responsible for limiting the short circuit current and fill factor of the device. The I-V characteristics for a silicon cell are plotted in figure 2.14a [5], the influence of series resistance (with ideal shunt resistance) can be seen to have an adverse effect on the fill factor and short circuit current.

Leakage or shorting paths between the n and p-type regions lead to the parallel or shunt resistance, R_{sh} . The shunt resistance should ideally be infinite but in practice shunt resistances of at least 100 Ohms are considered acceptable, as can be seen in figure 2.14b [5]. Low shunt resistance affects the open circuit voltage and fill factor of the device.

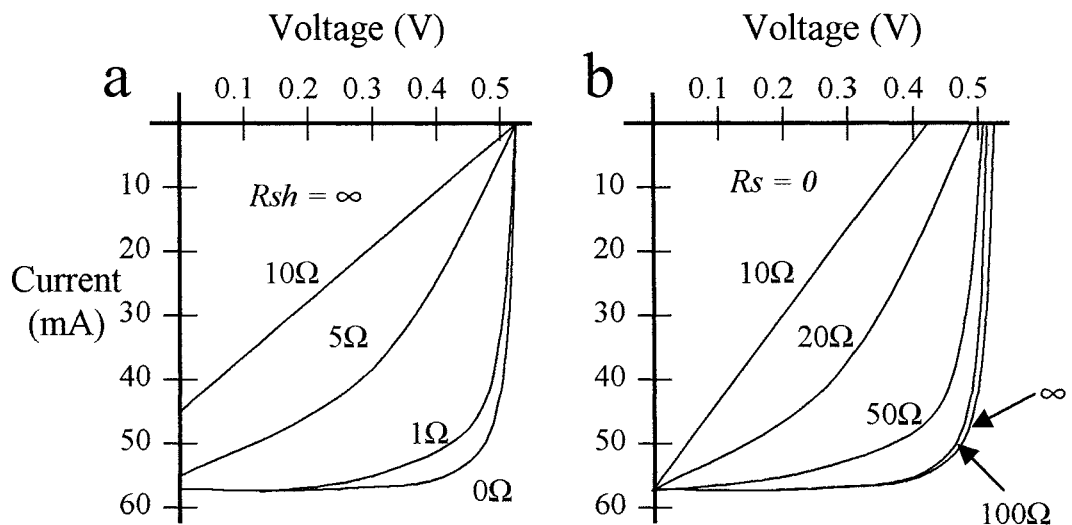


Figure 2.14. The Effects of Resistance on a Silicon Solar Cell
(a) Series Resistance and (b) Shunt Resistance [5]

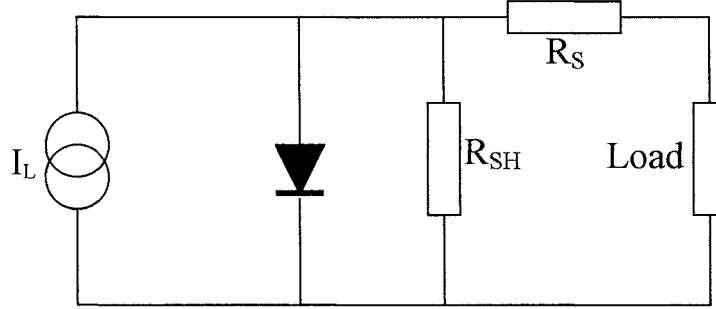


Figure 2.15. Equivalent Circuit of a Non-Ideal Solar Cell [6].

The equivalent circuit diagram of real solar cell, which takes into consideration the series and shunt resistances is shown in figure 2.15 [6]. In addition the current-voltage equation 2.44 is altered with regard to the device resistance and takes the form [1]

$$I = I_o \left(\exp^{\frac{e(V - IR_S)}{AKT}} - 1 \right) + \left(\frac{V - IR_S}{R_{SH}} \right) - I_L \quad 2.51.$$

Photons with energies just larger than the energy bandgap are generally absorbed a short distance into the material, whereas longer wavelength photons are absorbed further in the material. Providing these carriers are separated and pushed to an external circuit they will contribute to the total light generated current of the solar cell device. The sum of current contribution at each wavelength is the spectral response of a solar cell and the total sum across all wavelengths is the light generated photocurrent or short circuit current. The amount of carrier generation at each wavelength is an indication of the contribution of each region of the solar cell. By definition the spectral response, SR, for a solar cell is the ratio of the photo-generated carriers to the light incident upon the cell.

$$SR = \frac{J_L}{P_\lambda} \quad 2.52.$$

The quantum efficiency is a particular form of spectral response. The internal quantum efficiency, QE_{int} , is the number of photocarriers generated to the number of photons entering the material [6]

$$QE_{\text{int}} = \frac{J_L(\lambda)}{eF(\lambda)[1 - R(\lambda)]} \quad 2.53.$$

where $F(\lambda)$ is the photon flux entering the layer, $J_L(\lambda)$ is the total photocurrent density with contributions from the n-type, p-type and depletion region and $1-R$ is a correction for reflection loss at the front surface and interfaces. The ideal internal quantum efficiency is zero for photon energies smaller than the bandgap ($h\nu < E_g$) and unity for energies larger than the bandgap ($h\nu > E_g$). The external quantum efficiency, QE_{ext} , is the internal QE adjusted for reflection from the device surface [6]

$$QE_{\text{ext}} = QE_{\text{int}}[1 - R(\lambda)] \quad 2.54.$$

Once the quantum efficiency is known, integration over the wavelength range of interest gives the total photocurrent density obtained from the solar spectral distribution [5]

$$J_L = e \int_0^{\lambda_m} F(\lambda) QE_{\text{ext}}(\lambda) d\lambda \quad 2.55.$$

where λ_m corresponds to the semiconductor bandgap. To obtain the maximum photocurrent density, $R(\lambda)$ should at a minimum (ideally zero) and the $QE_{\text{ext}}(\lambda)$ a maximum (ideally unity) over the wavelength range $0 < \lambda < \lambda_m$.

2.3 The Ideal Heterojunction

Heterojunctions are the result of two dissimilar semiconductor materials brought into immediate contact to form a junction. The abrupt heterojunction comes in two different formats; the anisotype, in which the two semiconductor materials have different conductivity types (i.e. n and p-type) and are minority carrier devices, similar to the ideal homojunction. The second is the isotype heterojunction, which is formed by semiconductors of the same conductivity type (i.e. n-n and p-p types) and unlike the anisotype heterojunction (and homojunction), the minority carrier influence is insignificant, therefore these are classed as majority carrier devices. In many heterojunction solar cells (including all the solar cells manufactured in this work) a small bandgap absorber material (generally p-type) is coupled to a large band-gap window material (generally n-type).

A method for representing the energy band diagram of a heterojunction was developed by Anderson [9]. This approach was to class the heterojunction by the semiconductor characteristic constituent elements, namely by their bandgap, E_g , work function, ϕ , and electron affinity, χ . The work function is defined as the energy required to remove an electron from the Fermi level to the vacuum level, whereas the electron affinity is the energy required to remove an electron from the bottom of the conduction band to the vacuum level. Figure 2.16a shows the two semiconductors prior to junction formation and figure 2.16b shows the junction after formation. Note: the postscripts n and p refer to the n and p-type materials respectfully rather than the electrons and holes. Upon making contact, the Fermi levels of the two semiconductors are aligned by the transfer of electrons.

The Anderson model, like the ideal p-n homojunction, maintains that the semiconductor interface should be abrupt. However, this model does not take into consideration the effects of dipoles and interface states. The two factors that can be considered constant for the individual semiconductors are their energy bandgap, E_g , and electron affinity, χ . The work function however, is dependent upon the level of doping and for an n-type semiconductor can be given by

$$\phi_n = \chi_n + \delta_n \quad 2.56.$$

where δ_n is the energy separation between the Fermi level and the conduction band edge.

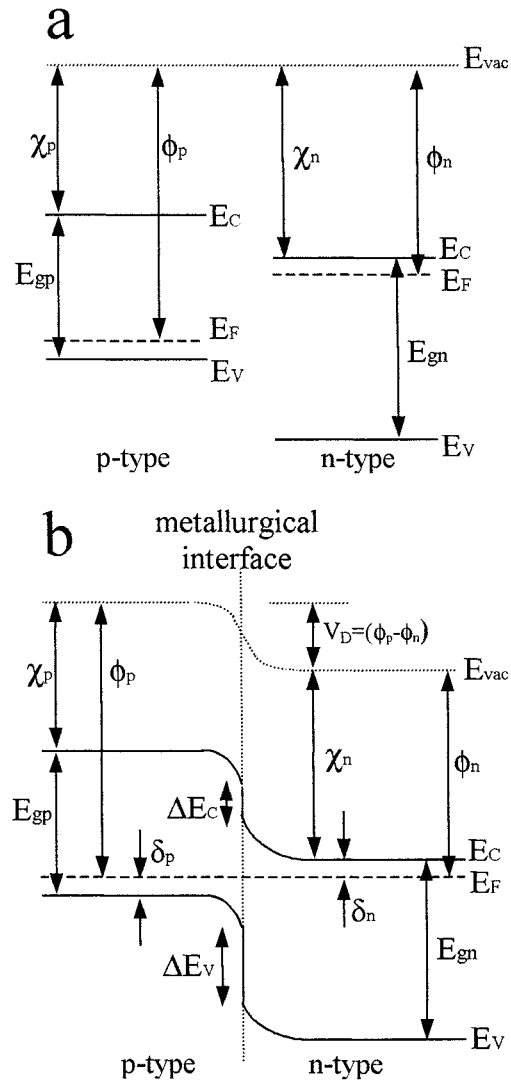


Figure 2.16. Anderson Energy Band Model of a p-n Heterojunction
(a) Before Junction Formation and (b) After Formation

For an n-type non-degenerate semiconductor, this separation can be written as [5]

$$\delta_n = \left(\frac{-kT}{e} \right) \ln \left(\frac{N_D}{N_C} \right) \quad 2.57.$$

where N_D is the concentration of donors and N_C is the effective density of states at the conduction bandedge. Conversely, for a p-type semiconductor, the work function is given by

$$\phi_p = \chi_p + Eg_p - \delta_p \quad 2.58.$$

and δ_p in this case is the separation between the valance bandedge and the Fermi level. Again for a non-degenerate p-type semiconductor, δ_p is given by [5]

$$\delta_p = \left(\frac{-kT}{e} \right) \ln \left(\frac{N_A}{N_V} \right) \quad 2.59.$$

where N_A and N_V are the acceptor concentration and effective density of states at the valance bandedge respectively. The discontinuity in the conduction bandedge (ΔE_c) is equal to the difference in electron affinities and is given by [7]

$$\Delta E_c = \chi_p - \chi_n \quad 2.60.$$

The discontinuity in the valance band is a function of not only the electron affinities, but also the energy bandgaps of both semiconductor materials. ΔE_v can therefore be written as [7]

$$\Delta E_v = (Eg_n - Eg_p) - \Delta E_c \quad 2.61.$$

The built-in voltage (V_D) is due to the difference in work functions.

$$V_D = \phi_p - \phi_n \quad 2.62.$$

or [7]

$$V_D = Eg_p + \Delta E_c - \delta_p - \delta_n \quad 2.63.$$

Since interface states are not present in this model, a depletion region is formed either side of the junction, therefore the width of this region can be obtained by solving Poisson's equation on either side of the boundary [5]

$$x_p = \sqrt{\frac{2\epsilon_n\epsilon_p N_D V_D}{eN_A(\epsilon_n N_D + \epsilon_p N_A)}} \quad 2.64.$$

$$x_n = \sqrt{\frac{2\epsilon_n\epsilon_p N_A V_D}{eN_D(\epsilon_n N_D + \epsilon_p N_A)}} \quad 2.65.$$

and the total depletion width is given by

$$W = x_p + x_n = \sqrt{\frac{2\epsilon_n\epsilon_p V_D (N_A + N_D)^2}{eN_A N_D (\epsilon_n N_D + \epsilon_p N_A)}} \quad 2.66.$$

If the single sided junction approximation is used where $N_D \gg N_A$ then the depletion region width is approximated to

$$W = \sqrt{\frac{2\epsilon_p V_D}{eN_A}} \quad 2.67.$$

which is the same result as found for the single sided homojunction, equation 2.11. Anderson also derived an equation for junction capacitance (per unit area) by again extending the homojunction theory [7]

$$C_J = \sqrt{\frac{e\epsilon_n\epsilon_p N_A N_D}{2(\epsilon_n N_D + \epsilon_p N_A)V_D}} \quad 2.68.$$

and again using single sided junction approximation for $N_D \gg N_A$ this can be reduced to

$$C_J = \sqrt{\frac{e\epsilon_s N_A}{2V_D}} \quad 2.69.$$

which is the same as equation 2.14 for the single sided homojunction. The Anderson model for the band profile of figure 2.16 predicts a current density-voltage relation of [10,11]

$$J = J_{00} \exp\left[-\frac{e(\Delta E_c + V_D)}{kT}\right] \times \left[\exp\left(\frac{eV}{kT}\right) - 1\right] \quad 2.70.$$

under a bias, V , where

$$J_{00} = eXN_D \sqrt{\frac{D_n}{\tau_n}} \quad 2.71.$$

where X is the transmission coefficient for electrons to cross the interface, D_n is the minority carrier diffusion coefficient and τ_n is the minority carrier lifetime of the electrons in the p-type material.

2.3.1 Dark Current Characteristics of the Heterojunction

The dark current characteristic models of a heterojunction are in essence modifications or extensions of homojunction theory. These current transport mechanisms are covered in more detail by (Hovel ch 6 [6], Mitchell ch 2 [7], Milnes and Feucht ch 2 [10] and Sharma and Purohit ch 1 [11]).

2.3.1.1 The Anderson Diffusion Model

The Anderson model uses the energy band profile to determine the barrier heights at the metallurgical interface. In having differing semiconductor parameters such as electron affinity, energy bandgap and work function, the formation of the junction does not always result in smooth band profile such as that shown in figure 2.16. The consequence of this is the possible formation of notches and spikes in the conduction and valence bands, which lead to energy barriers for the collected carriers. For example is the case where $\chi_p > \chi_n$, $\phi_p > \phi_n$ and $\chi_p + E_{gp} < \chi_n + E_{gn}$ a distortion leading to a spike and notch in the conduction band is found as shown in figure 2.17. The barrier in the conduction band, ΔE_c , is still the difference in the electron affinities and the diffusion potential, V_D , is the difference in the work functions but also the sum of the potentials either side of the junction ($V_D = V_{Dp} + V_{Dn}$). The relationship between the semiconductors built in voltages is given by [10]

$$\frac{V_{Dp}}{V_{Dn}} = \frac{N_{Dn}\epsilon_n}{N_{Ap}\epsilon_p} \quad 2.72.$$

where ϵ_n and ϵ_p are the dielectric constants of the n and p-type semiconductors respectively.

The Anderson model predicts that due to interface distortions, the diffusion current will consist mainly of carriers that overcome the smallest barrier. Since the hole barrier for the heterojunction shown in figure 2.17 is larger, then the electrons will be the dominant carrier. The current density-voltage characteristics of this band profile (ignoring the generation-recombination current) is given by [10,11]

$$J = J_{00} \exp\left[-\frac{e(V_D - \Delta E_C)}{kT}\right] \times \left[\exp\left(\frac{eV}{kT}\right) - 1\right] \quad 2.73.$$

where J_{00} is the same as equation 2.71,

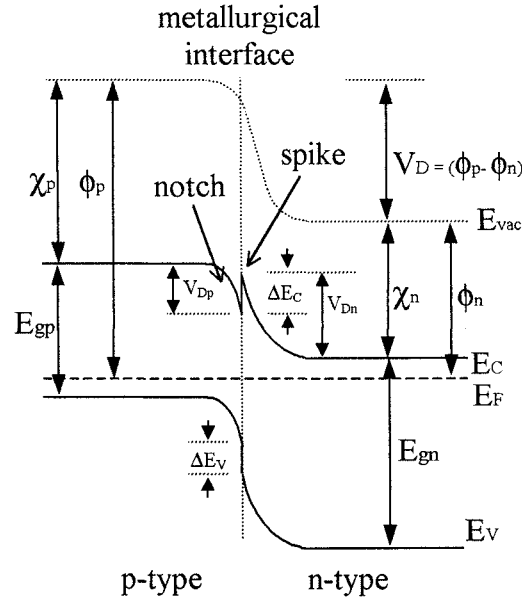


Figure 2.17. Anderson Energy Band Model of an Abrupt p-n Heterojunction, Showing Band Distortions

The Anderson model is commonly used to develop band profiles and their current mechanism but the experimental results for the temperature dependence and voltages do not always agree with the theoretical. In addition, Anderson tried to compensate for the discrepancy of lower currents in experimental results by including the transmission coefficient, X (of equation 2.71). It was assumed that reflection of

carriers at the interface was the cause of the lower current and therefore a lower value of X is required to match the experimental results.

2.3.1.2 The Emission Model

The problems encountered with the transmission coefficient of the Anderson model are on the whole avoided by the emission model of Perlman and Feucht [12]. Unlike Anderson's, this model includes the effects due to the conduction band spike. They assumed, for an abrupt p-n heterojunction where electrons are the main transport carriers, two modes of J-V operation exist; (a) homojunction, where the current passage is limited by a minority carrier build up at the edges of the depletion region and (b) metal – semiconductor, where the current is in this case restricted by a potential barrier on the n-side of the junction. When the spike lies below the conduction band of the p-side, the homojunction type process dominates, whereas the metal-semiconductor type process dominates when there is a large reverse potential barrier, V_R , as shown in figure 2.18.

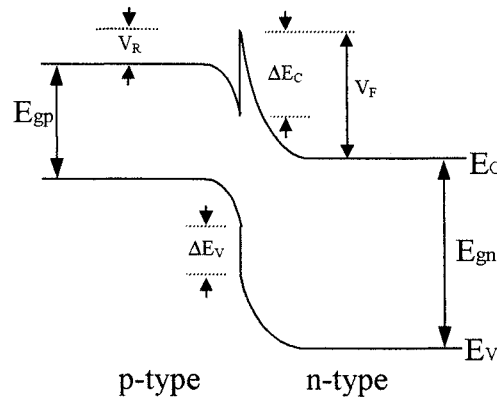


Figure 2.18. Energy Band Diagram of the Emission Model of an Abrupt p-n Heterojunction

The J-V characteristics (neglecting space charge generation-recombination) are given by [12]

$$J = J_o (\exp^{eV/kT} - 1) \quad 2.74.$$

where J_o for the homojunction type dominating behaviour is given by

$$J_o = eN_D \sqrt{\frac{D_n}{\tau_n}} \quad 2.75.$$

and where the metal – semiconductor type behaviour dominates is given by

$$J_o = 1/2 eX_m N_D \sqrt{\frac{2kT}{\pi m_n^*}} \exp^{-e(V_F - V)/kT} \quad 2.76.$$

where m_n^* is the effective mass of the electrons in the n-type material and V_F is the forward barrier height.

2.3.1.3 The Emission - Recombination Model

A model that considers the effects of interface states was proposed by Dolega [11]. This model assumes there is fast recombination of electrons and holes via thermal emission in a thin layer at the metallurgical interface. It was also assumed that no rectification would take place as long as the interface width is narrower than the space charge region. In this model, the p-n heterojunction appears to act as two metal-semiconductor contacts in series with the bias voltage controlling the boundary conditions of the current carriers. The forward J-V characteristics were rewritten to give a simplified expression

$$J = J_o (\exp^{eV/nkT} - 1) \quad 2.77.$$

and

$$J_o = J_{oo} \exp^{(-eV_D/nkT)} \quad 2.78.$$

where the term J_{oo} is a weak function of temperature. Also in forward bias, the diode factor (for heterojunctions) n is dependant upon the densities of semiconductor imperfections and varies between 1 and 2 (i.e. between $\exp^{(eV/kT)}$ and $\exp^{(eV/2kT)}$). The homojunction recombination model of section 2.2.3.2 (Sah-Noyce-Shockley) can then be used to approximate the space charge region current.

2.3.1.4 The Tunnelling Model

A model to describe tunnelling through the barrier of an abrupt p-n heterojunction was introduced by Rediker et al [11]. Using a similar band profile to that of figure 2.18, electrons in the conduction band either have to tunnel through or surmount the potential barrier to cross the junction. The type of forward bias mechanism is ultimately dependant upon the material properties of the n-type layer.

The tunnelling current is obtained from the product of the incident electron flux and the expression for the tunnelling probability, T . When tunnelling through the barrier is much larger than thermal emission over the barrier, the J-V characteristics can be written as

$$J = J_o(T) \exp^{(V/V_o)} \quad 2.79.$$

where $J_o(T)$ varies weakly with temperature and V_o is a constant.

An expression for the temperature dependence could not be established. However, experiments on the forward currents of p-n heterojunctions showed that the an empirical relationship proportional to $\exp^{(T/T_o)}$ could be found. This allowed equation 2.79 to be rewritten as

$$J = J_{oo} \exp^{(T/T_o)} \exp^{(V/V_o)} \quad 2.80.$$

where J_{oo} , T_o and J_o are all constants.

From the experimental relationship, the voltage and temperature were shown to be independent variables but the temperature dependence was exponential.

2.3.1.5 The Tunnelling - Recombination Model

A model by Riben [11] proposed interband tunnelling in conjunction with recombination. For the p-n heterojunction of figure 2.19 electrons from conduction band of the n-type material tunnel into free interband states of the p-type material where they combine with holes. An analogous process is found for holes from the p-type material combining with electrons. For tunnelling originating at the bottom of the conduction band, the forward current density takes the form

$$J = B \exp^{[-\alpha(V_D - V)]} \quad 2.81.$$

where B is a weak function of voltage and temperature and V is the applied voltage. The α term consists of the effective mass, dielectric constant and carrier concentration but is also related to the barrier shape. Where the barrier is classed as linear, a constant field in the transition region with position is found. If tunnelling is limited to mostly the n-region then α is given by

$$\alpha = \frac{4}{3\hbar} \sqrt{\frac{m_n^* \epsilon_n}{N_D}} \quad 2.82.$$

or for tunnelling mostly in the p-region

$$\alpha = \frac{4}{3\hbar} \sqrt{\frac{m_p^* \epsilon_p}{N_A}} \quad 2.83.$$

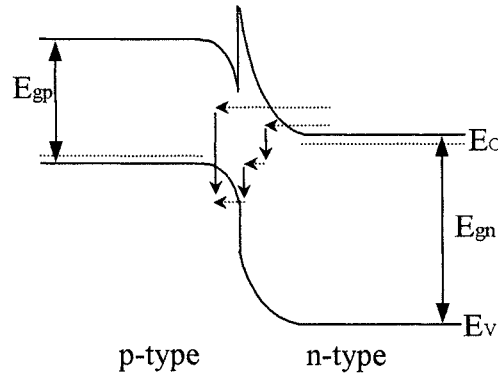


Figure 2.19. Energy Band Diagram of the Tunnelling-Recombination Model of a Forward Biased Abrupt pn Heterojunction, Showing Multi and Single Step Processes.

If the assumption is made that the n-region is more heavily doped than the p-region ($N_D \gg N_A$) the forward tunnelling current density can be expressed as [11]

$$J = J_o \exp(\alpha K_p V) \quad 2.84.$$

with

$$J_o = B X N_t \exp(-\alpha V_D) \quad 2.85.$$

and

$$K_p = \left(1 + \frac{N_A \epsilon_p}{N_D \epsilon_n} \right)^{-1} \quad 2.86.$$

where α is given in equation 2.83, V_D is given in equation 2.63, B is a constant and N_t is the density of states available for tunnelling. This tunnelling current density can also be written as [11]

$$J = J_{oo} \exp^{(\beta T)} \exp^{(\alpha K_p V)} \quad 2.87.$$

the β term shows the effect of the temperature coefficient of the diffusion voltage [7]

$$\beta = -\alpha \left(\frac{\partial E_{gp}}{\partial T} + \frac{\partial \Delta E_V}{\partial T} - \frac{\partial \delta_n}{\partial T} - \frac{\partial \delta_p}{\partial T} \right) \quad 2.88.$$

Adirovich [13] used the multi-step tunnelling-recombination model to explain the dark current mechanism of an n-CdS / p-CdTe thin film heterojunction. For multi-step tunnelling, the α term is modified to take into consideration the number of tunnelling steps, R

$$\alpha^* = \frac{\alpha}{\sqrt{R}} \quad 2.89.$$

2.3.1.6 Overview of Heterojunction Dark Current Models

Anderson placed the heterojunction models of other workers into two groups by virtue of their thermal nature, in an attempt to find an explanation for the I-V characteristics as a function of applied voltage. The first group proposed by Anderson is thermal currents in which to cross the junction, the current carriers must overcome the potential barrier, and can be generally expressed in terms of current density, by [11]

$$J = J_{oo} \exp^{-\phi/kT} \exp^{eV/nkT} \quad 2.90.$$

where ϕ is the activation energy or barrier height with no applied bias and J_{oo} is a constant determined by the model. The diffusion, emission and emission-recombination models (sections 2.3.1.1, 2.3.1.2 and 2.3.1.3) can all be expressed by equation 2.90 in terms of their thermal currents.

The second group classed as non-thermal, occur when current-carriers tunnel through the base of the potential barrier or spike. Examples of this are the tunnelling and tunnelling-recombination models of sections 2.3.1.4 and 2.3.1.5. However, a third type or amalgamation of the previous two explanations can occur. The current carrier can partially surmount but then tunnels through the potential barrier. In this case the tunnelling currents should be classed as thermal in nature.

2.4 Semiconductor to Metal Contacts

When a metal and semiconductor are brought together, as with the p-n junction, the Fermi level must remain constant throughout the interface, requiring an exchange of electrons (and holes) producing band bending. Commonly, such contacts are found to be either rectifying or Ohmic. Rectifying or Schottky barrier contacts generate a depletion region in the semiconductor, thus limiting current flow in one direction and preventing carrier injection in the other. However, Ohmic contacts form an accumulation layer of carriers in the semiconductor, which allows current to flow in either direction. Figure 2.20 [4] shows the energy band diagram of a metal to n-type semiconductor junction, before and after contact, for both rectifying and Ohmic junctions.

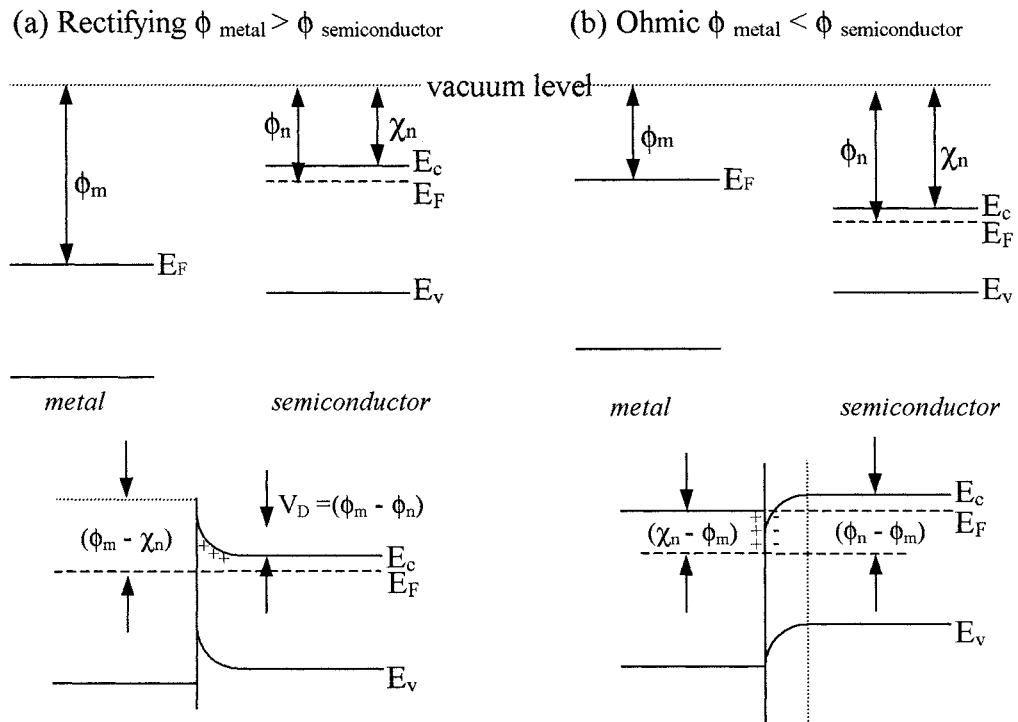


Figure 2.20. Energy Band Diagrams of a Metal to n-type Semiconductor Junction, Before and After for (a) Rectifying and (b) Ohmic Contacts [4]

In making contacts to solar cells, the metal-semiconductor junction should not restrict current flow and therefore an Ohmic contact is favoured. For metal to n-type semiconductor junction an Ohmic contact is formed when the work function of the metal is smaller than the semiconductor ($\phi_m < \phi_n$). In the case of a metal to p-type

junction, the work function of the metal is larger than the semiconductor ($\phi_m > \phi_p$). Unfortunately, Ohmic contacts can in some cases be difficult to achieve (as in the case of p-CdTe to metal, discussed in chapter 3) and the current mechanisms across the rectifying junction need to be considered. To form a metal to n-type rectifying junction, the metal work function needs to be larger than the semiconductor ($\phi_m > \phi_n$) and smaller for the metal to p-type ($\phi_m < \phi_p$). In forming the rectifying junction, a contact potential, V_D , is produced and is given by

$$V_D = \phi_m - \phi_n \quad 2.91.$$

for the metal to n-type semiconductor. For the metal to p-type semiconductor the contact potential is given by

$$V_D = \phi_p - \phi_m \quad 2.92.$$

Unlike a p-n junction, the current transport of the metal-semiconductor junction is mainly due to majority carriers. Sze (ch 5) [5] describes four types of current mechanisms under forward bias, in many ways similar to the transport theory of the p-n junction; (1) transport of electrons from the semiconductor to metal over the potential barrier. (2) Tunnelling of electrons through the potential barrier. (3) Space-charge region recombination and (4) metal to semiconductor hole injection.

In the work of Kurtin et. al. (In Sze ch 5, [5]) they attempted to determine the work functions of various semiconductors. It was shown that ionic semiconductors obeyed the simple rules and a correlation between interface behaviour and metal electronegativity (or the work function) was determined (i.e. CdS and ZnS). However, semiconductors with covalent bonds did not always obey this rule and were prone to Fermi level pinning due to surface states (i.e. most III-V compounds).

The definition of an Ohmic contact is a metal-semiconductor junction in which the contact resistance is insignificant compared to the bulk semiconductor resistance. In addition, any potential barrier should be much smaller than the potential barrier across the active region of the device. Sze has shown that in order to obtain low contact resistances, the semiconductor must be heavily doped which will allow

tunnelling to be the dominant process. Alternatively a low barrier height allows thermionic emission currents to dominate the transport process.

2.5 Material Properties

The structure and interface play an important role in performance of the heterojunction. Crucial to this are the material properties of the semiconductors and the metals, when used to create a device. Atomic bonds, with the two most important being the ionic and covalent bonds, hold atoms in a crystal lattice together. The ionic bond is a result of the mutual electrostatic attraction of ionised charges, where a covalent bond is found when valence electrons are shared between atoms. Atoms fixed in the lattice show long-range order, however, at the surface of a crystal, a large number of surface states can be introduced due to the lack of atoms to form bonds. Known as dangling bonds, these energy states can be the cause of high surface recombination.

The atoms in a perfect crystal are fixed in their specified atomic sites. Unfortunately this is not the case for real crystals. Extra, missing, misplaced or abnormal groupings of atoms can cause defects in the crystal structure. The simplest form of crystal imperfection is the point defect. When an atom is missing from the lattice it is called a vacancy. A foreign atom that replaces a host atom in the lattice is called a substitutional impurity or on a non-atomic site, an interstitial impurity. In the case where an interstitial atom is a host atom adjacent to a vacancy, a Frenkel defect is found. Point defects cause local distortions in an otherwise perfect lattice, the amount of which is dependant upon the size of the atoms involved. Local distortions can increase the resistance of the crystal as they act as scattering centres to current flow. In addition, as a charge is normally associated with the point defect, they can act as traps for carriers.

A dislocation is a type of crystal imperfection in which a row of atoms is out of position and therefore are commonly called line defects. There are two basic types: edge and screw dislocations. The edge dislocation is the removal, or insertion, of an extra plane of atoms causing severe distortion in the local area. When a shear force is applied, the edge dislocation allows slipping in the crystal lattice. Screw dislocations can be visualised by a cut in a perfect crystal where one side of the cut is displaced

relative to the other and the atomic layers spiral around the dislocation. Edge and screw dislocations quite often occur together.

The third type is plane or area defects, which are effectively two-dimensional deficiencies and represent large discontinuities in the crystal lattice. The principal plane defect, which occurs in most materials, is the grain boundary. Polycrystalline solids do not always consist of a large single crystal but many crystallites. The divide between these crystallites is the grain boundary, with each grain possibly containing other line and point defects. Another plane defect is twining, describing a change in crystal orientation across a plane. The stacking fault is a plane defect that occurs when mistakes are made in the sequence of crystal plane stacking.

The final, three-dimensional defects are voids and inclusions. When dopants or impurities are introduced to the host lattice there is only a finite amount that the structure can accept during processing due to material solubility. However, when the structure is cooled, the amount the lattice is able to accept can reduce still further. To compensate for this, the precipitation of the dopants or impurities is found which results in dislocations of the host lattice.

In addition to the structural defects described thus far, phonons can be considered as crystal imperfections. Photon transitions involve atoms absorbing and emitting quanta of light, whereas analogous to this is the phonon and quanta of thermal energy. Any crystal lattice at an elevated temperature can be considered as three-dimensional oscillators, the energy of which is quantised, and therefore atoms are prone to phonon absorption.

In order to reduce the risk of lattice defects at the junction interface, lattice matching of the heterojunction partners is desired. The percentage of lattice mismatch can be calculated by [11]

$$Lattice\ mismatch = \frac{2(\lambda_1 - \lambda_2)}{(\lambda_1 + \lambda_2)} \quad 2.93.$$

where λ_1 and λ_2 are the lattice constants of the two semiconductors. For similar systems (i.e. either all wurtzite or all sphalerite) the lattice mismatch for the heterojunction partners used in this work are: CdTe/ CdS ~10%, CdTe/ ZnSe ~ 13% and CdTe/ ZnS ~ 18%. Bube et. al. [14] also calculated the lattice mismatch using the electron affinity of the semiconductors and found: CdTe/ CdS 9.7%, CdTe/ ZnSe

12.5% and CdTe/ ZnS 15.3%. Where lattice mismatch does occur, interface states can be expected which can be electrically active. As the lattice spacing of the heterojunction materials is different, dislocations in the form of dangling bonds can be found at the interface.

Where a large number of electrically active interface states exist, two heterojunction mechanisms exist [1] (1) the conduction band level at the interface is distorted relative to the Fermi level due to charge stored in the interface states. If a high concentration of the charged interface states exists at the junction, the Fermi level can be held at an artificial energy level. Known as Fermi level pinning, a distortion in the energy band can increase the barrier height of the conduction band, thus restricting carrier flow. (2) An increase in the reverse saturation current (I_0) is caused by the number of recombination sites available, which is shown as an increase in the recombination velocity.

Additional factors to be considered when selecting the heterojunction partners are thermal mismatch and interdiffusion. A thermal mismatch during processing can cause defects while cooling, which in extreme cases can result in coating breakdown. Interdiffusion of the semiconductor partners can be found when the coatings are processed at high temperatures, which may cause defects at the interface, or preferentially relax the mismatch between the partners.

2.6 Thin Film Solar Cells

When n-type CdS is deposited on SnO₂ coated glass and a p-type CdTe absorber layer is added, the device produced is said to be in the superstrate configuration. A diagram of this type of thin film solar cell is shown in figure 2.21. The SnO₂ coated glass window is used to form a transparent conducting base to which the buffer layer can be deposited. The buffer layer's function is to contribute to carrier production, compensate for the mismatches between the TCO and absorber layer, but also reduce interdiffusion between the two. This layer is normally less than 500nm thick and made from a material with an energy bandgap greater than the absorber layer. The p-type layer is thick enough (2 to 5 microns) to allow absorption of the incident photons and generate the current carriers. The rear contact of the device must

be Ohmic, to reduce the electrical barrier between the solar cell and the external circuit.

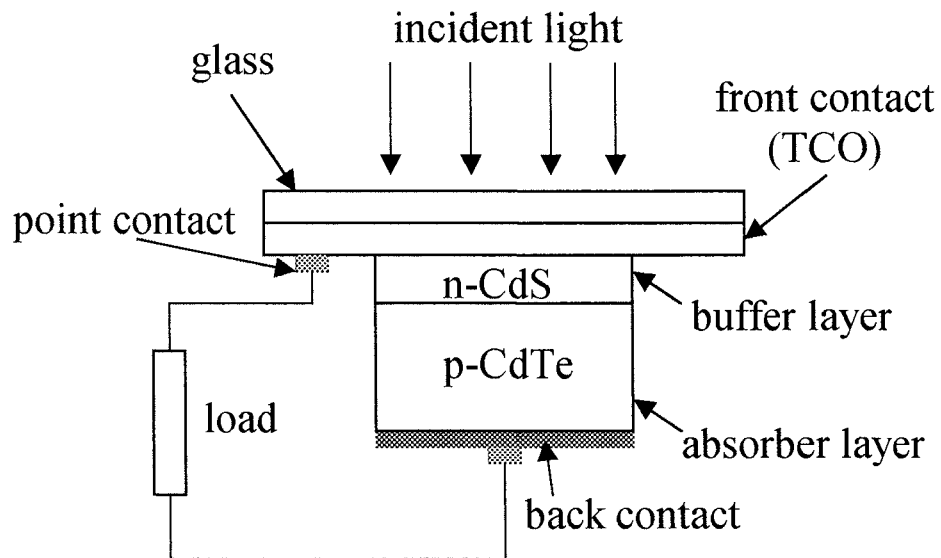


Figure 2.21 Diagram of a Superstrate Configuration CdS-CdTe Thin Film Solar Cell.

2.6.1 Properties of Polycrystalline Thin Films

Depositing thin films of semiconductor materials by low cost means generally leads to polycrystalline layers, in which a short-range order is found. Polycrystalline layers usually consist of many crystallites, which are separated by numerous grain boundaries. The grain boundaries are areas in which the minority carrier recombination velocity is increased. This leads to reduced photocurrent, increased dark current, lower shunt resistance and an increase in the series resistance [6]. The shape of the grains play an important role in how active the boundaries become in effecting the properties of the solar cell. If the layer consists of randomly orientated small grains that cut across the minority carrier paths, then an increase in the dark current of the cell due to large minority carrier recombination will be found. If however the grains are columnar and extend from the front to the back of the cell, the minority carriers have a much greater chance of contributing to the photocurrent. Diffusion down the grain boundaries during processing, can lead to shorting paths through the layers that will increase the shunt resistance of the device. The boundary between two grains can be modelled by a capacitance in parallel with a resistance that

is typically higher than the intergrain resistance [15] and accounts for the increased series resistance that is found with grain boundaries.

2.6.2 The Buffer Layer

A problem with the CdS layer is that it absorbs light below 510nm, thus reducing the ‘window of light’ that can pass through it. Other materials extensively investigated as alternatives to CdS are $\text{CdZn}_{1-x}\text{S}_x$ and ZnO (E_g of 3.35eV) [16]. In principle these will improve device efficiency by increasing the transmittance of light to the junction where more electron hole pairs will be generated. The nature of the interface is however altered by using other buffer materials and despite a smaller optical window, the CdS / CdTe devices have been produced with high efficiencies.

Buffer layer requirements are: -

1. The energy bandgap should be as large as possible to allow as many photons as possible to reach the junction and increase the possibility of absorption.
2. The buffer layer should be composed of densely packed crystallites with good crystallinity; the layers should also be free from pinholes.
3. This layer should couple the incident light into the absorber layer with a minimum of optical reflection and absorption.
4. The buffer layer resistivity should be sufficiently low so as not to cause series resistance problems.
5. There should be good lattice matching with the absorber layer to minimise stress at the interface and to minimise the density of dangling bonds.
6. The electron affinity should complement the absorber layer to avoid deleterious spikes and notches in the heterojunction interface.

2.6.3 The Absorber Layer

As discussed in Chapter 1, the ideal absorber layer energy bandgap is 1.5eV (for AM 1.5), therefore for maximum efficiency, an absorber layer with an energy bandgap between 1.1 and 1.7eV is required. Another consideration is bandgap type, as light absorption is much weaker in an indirect bandgap semiconductor than in a direct bandgap semiconductor.

Absorber layer requirements are: -

1. The semiconductor should have a band gap as near to 1.5 eV as possible to allow a significant part of the wide spectrum of the sunlight to be absorbed.
2. The layer should be p- type as the minority carrier diffusion length of electrons (in p-type material) is longer than holes (in n-type material).
3. The minority carrier diffusion length should be greater than $1/\text{absorption coefficient}$ to ensure the excess minority carriers reach the junction without excessive losses due to recombination. This means that the minority carrier lifetime and mobility should be as high as possible.
4. The resistivity of the absorber layer should be sufficiently low to avoid series resistance problems.
5. Large, densely packed grains are desired, which reduces the losses due to recombination at the grain boundaries.

2.6.4 Back Contacts

A good Ohmic contact is required between the back contact and the absorber layer. However, due to its high work function and problems in production of low resistive thin films, Ohmic contacts to p-CdTe are difficult.

Back contact requirements are: -

1. The junction between the absorber layer and metal back contact must be Ohmic.
2. Methods to achieve an Ohmic contact are: -
 - (i) The use of a metal with a higher work function than the absorber layer.
 - (ii) The formation of a p^+ region under the contact by the reaction or interdiffusion of a dopant to reduce the barrier width, which will permit quantum tunnelling through the barrier.
 - (iii) By surface treatment using etches to adjust the surface stoichiometry and leave a cadmium-depleted region. The Te rich surface can then be used to react with the contact and enhance diffusion into the surface.

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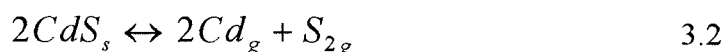
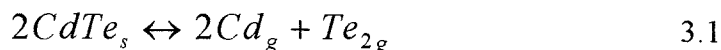
Chapter Three

Literature Review

3.1 Deposition Techniques

3.1.1. Close Spaced Sublimation (CSS)

Close spaced sublimation has been used extensively for the deposition of CdTe and CdS thin films. This technique is based on the reversible dissociation of compounds at high temperature, for example [1].



The CSS process involves heating the source compound to a higher temperature than the substrate. At a high enough temperature, the source dissociates into its elements which recombine on the substrate, depositing the source materials as a thin film. The distance between the source and substrate is small, generally less than a few millimetres. Also with the source-substrate distance being less than a few percent of the substrate dimensions, the material transport conditions are said to be independent of the system conditions. Direct transport of each component across the opening is achieved due to the small spacing between the source and substrate. Early epitaxial growth of III-IV compounds using close spaced chemical vapour transport is similar to CSS, however in this case, no transport agent is used.

A schematic diagram of the deposition apparatus is shown in figure 3.1. Due to the proximity between source and substrate, a baffle arrangement is sometimes used to prevent spitting of the source compound, which produce “pinholes” in the deposited layer. The CSS technique uses a chamber pressurised with an inert gas (Ar or He). Altering the source and substrate temperatures and changing the distance between them or the baffle arrangement can alter the growth rate and microstructure of the coatings. The chamber ambient controls the mean free path of the gaseous species. At high pressures, the mean free path is small and the condensation process is comparable to the distance between the source and substrate. The material utilisation is high and with the substrate temperature controlling the growth rate, deposition on less sturdy substrates at elevated temperatures can be achieved.

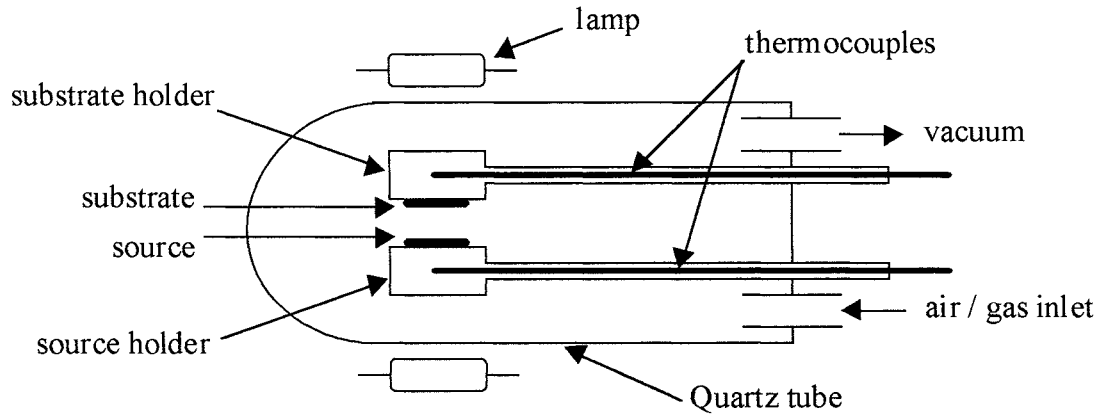


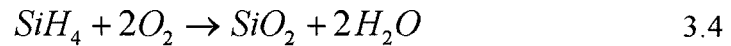
Figure 3.1. Schematic Diagram of a Close Spaced Sublimation Apparatus (CSS).

3.1.2. Chemical Vapour Deposition (CVD)

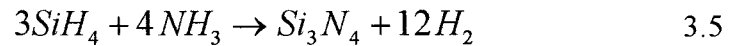
If a substrate is placed in a permanent gas flow with, for example, a combination of A B vapours, then this reaction can be described by



Similar reactions can be found for silicon dioxide with a N_2 carrier gas,



or silicon nitride,



or even polysilicon,



The CVD technique allows precise control of the layer's stoichiometry and doping concentrations. A stability constant $K(T)$ can be used to characterise the process described in the reaction equations. The stability constant at equilibrium for a given temperature is,

$$K_{AB(T)} = (p_A^0)(p_B^0)^{1/2} \quad 3.7$$

where P_A^0 and P_B^0 are the equilibrium partial pressures at temperature T [1].

A diagram of the deposition system is shown in figure 3.2. Inside the quartz tube is the cadmium, tellurium and a substrate. A multi-zone furnace allows the substrate temperature to be kept higher than that of the source chemicals. A carrier gas of H_2 or He conveys the vapours to the heated substrate where the deposition takes place. The reaction mixture (i.e. stoichiometry) of the coating is dependent upon the substrate temperature, whereas the partial pressures of the source materials (i.e. Cd and Te_2) control the deposition rate. In the case of CdTe, the electrical resistivity can be controlled by altering the stoichiometry, varying the Cd-Te ratio, or by extrinsic doping using PH_3 or AsH_3 in the mixture.

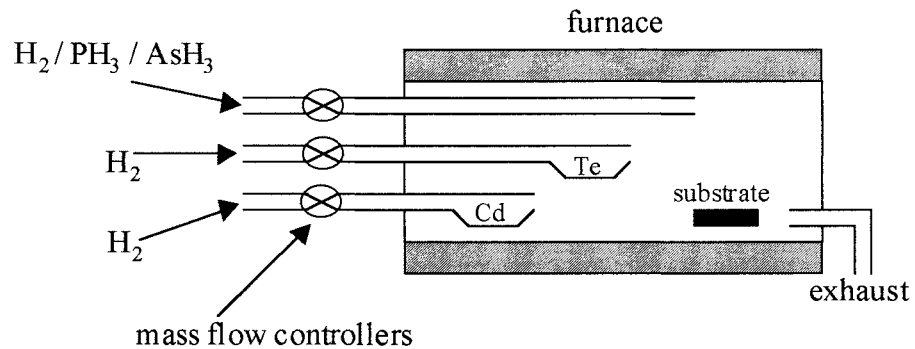
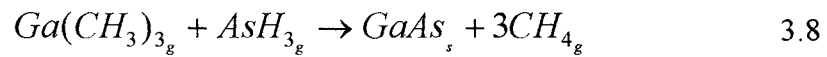


Figure 3.2. Schematic Diagram of a CVD System.

3.1.3. Metal Organic Chemical Vapour Deposition (MOCVD)

The term “metal organic” when added to CVD, refers to the gaseous mixtures used as source materials. Both CVD and MOCVD systems feed gases over a heated substrate. However, MOCVD organic gases such as dimethylcadmium or dimethyletellurium, are used as sources of cadmium and tellurium [2]. The reaction vessel remains cold and only the substrate is heated. MOCVD has been used extensively for III-IV crystal growth. When the gas mixture passes over the heated substrate, a reaction occurs on its surface. The reaction for GaAs, for example, is given by



3.1.4 Epitaxial Growth Methods

As with other deposition methods, epitaxial growth allows heterojunctions to be fabricated. However, the enhanced purity of the epilayers can give rise to better semiconductor properties (i.e. higher mobility, and better minority carrier lifetime and diffusion length). The principle behind epitaxial growth is to use a single crystal wafer as a seed of the material that you wish to cultivate, to which a new higher-grade layer with the same crystalline structure is grown.

3.1.4.1. Liquid Phase Epitaxy (LPE)

The three main LPE processes are shown schematically in figure 3.3. If the dipping process is considered (a), the polished substrate, or seed, is immersed in the molten semiconductor material. The substrate is then slowly withdrawn to a cooler zone of the furnace. By controlling the withdrawal rate and hence, temperature, a crystalline epitaxial layer is formed on the substrate. Adding impurities to the concentration can lower the melting point of the molten material. For example, when a GaAs substrate is dipped into GaAs+Ga the seed does not melt, therefore by controlling the rate of cooling, an epitaxial layer of GaAs is produced. The dipping process can be used to grow thick layers with a high throughput, however the

thickness control of thin layers can be difficult. The sliding boat method permits large area thickness control but can sometimes be difficult to grow and is also expensive, whereas tipping allows good thickness control but scale-up costs can again be prohibitive.

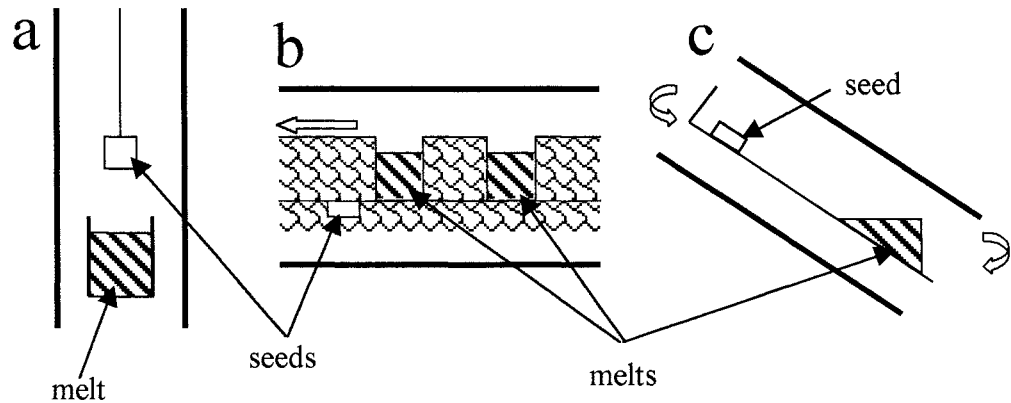


Figure 3.3. Schematic Diagram Different LPE Systems
(a) Dipping, (b) Sliding Boat and (c) Tipping.

3.1.4.2. Molecular Beam Epitaxy (MBE)

MBE is the co-evaporation of the elements in which no expense has been spared in the procurement of the deposition system, schematically shown in figure 3.4. Inside an ultra high vacuum (UHV), a directed beam of atoms (or molecules) is allowed to condense on the heated substrate, forming an epitaxial layer. A mass spectrometer analyses the vapour species and a reflection electron diffraction camera is used to monitor layer crystallinity. More sophisticated systems include a secondary ion mass spectrometer (SIMS) and Auger microprobes. The growth rate is very slow, $< 1\mu\text{m} / \text{hr}$ and this allows precise control of multi-layer thickness. Due to its sophistication, MBE is an expensive deposition technique. However, the quality and control of the process makes MBE one of the best systems for research-based semiconductor devices.

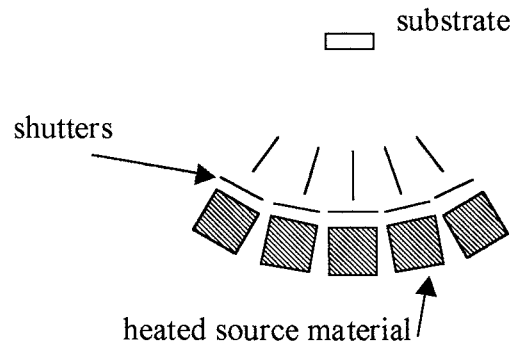


Figure 3.4. Molecular Beam Epitaxy (MBE) Apparatus.

3.1.5 Sputtering

Sputtering is the impact of ions or atoms on a solids surface that results in the ejection of an atom. The surface in question is known as the target or cathode. The resultant sputtered atoms condense onto a substrate to form a thin film. Many sputtering systems are available but the simplest and most common is glow discharge sputtering (a low temperature plasma), generated using a dc electric field. The discharge occurs in a partial pressure of approximately 10^{-2} mbar. The sample is placed on the anode and by applying an electrical potential, (a few kV) the ejected ions are accelerated from the cathode and condense on the substrate. The most familiar electrode configuration is where the cathode and anode are positioned parallel to one another. Other set-ups include cylindrical or wire cathodes and simultaneous sputtering can be realised using multiple targets.

An alternative method to glow discharge is magnetron sputtering. This process uses magnets to increase the ionisation efficiency. In addition, r. f. (radio frequency) sputtering allows non-metallic targets to be used, which is extremely useful in semiconductor material deposition. When using a dc supply and insulating target, a build-up of charge on the surface of the cathode prevents sputtering. This can be overcome by using a high frequency ac potential that neutralises the target surface. R.f. sputtering can be used in either glow discharge or magnetron sputtering systems.

3.1.6 Screen Printing

In this process, outlined in figure 3.5, a screen or plate containing the desired pattern is used to deposit the coating onto the substrate using a procedure commonly used in arts and crafts. The coating is in the form of a paste, which consists of three constituents, a fine metallic (or semiconductor) powder, a bonding agent and an organic suspension medium. For a typical solar cell, the paste for the window layer contains CdS, CdCl₂ and propyleneglycol (PG), whereas for the absorber layer CdTe replaces CdS [3]. The first stage of the printing process is to align the substrate with the screen mesh. Photolithography is used to outline areas on the screen and corresponds to locations where a coating (thin film) is required. The paste is dispensed on the upper surface of the screen and pressure is applied to the squeegee. This pushes the screen onto the substrate and by moving the carriage, the paste is forced through the mesh. After the squeegee has passed, tension between the screen and its frame forces it upwards, leaving a thin film on the substrate surface. Post deposition drying and heat treatment completes the layer fabrication.

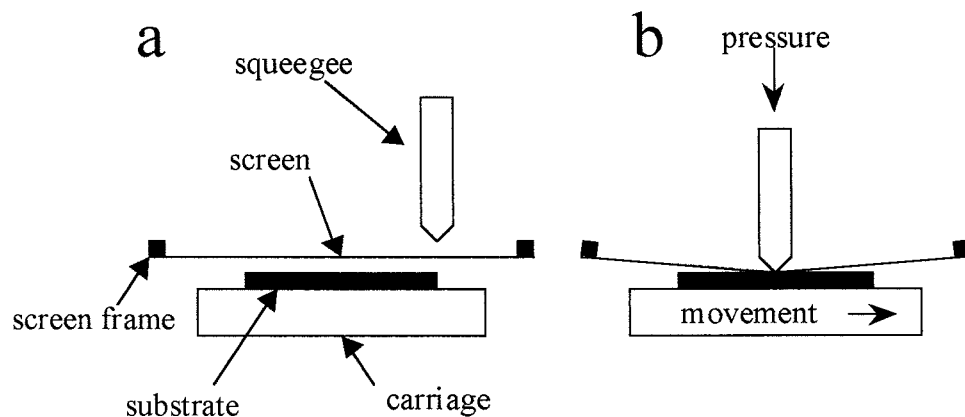


Figure 3.5. Schematic Diagram of Screen Printing Process,
(a) before and (b) during Deposition.

3.1.7 Spray Pyrolysis

This deposition process uses a spray to deposit a film onto a heated substrate, schematically represented in figure 3.6. The spray consists of a solution that reacts on the surface of the heated substrate to permit layer formation and the carrier gas, which is volatile at the spray temperature. The pressurised solution and carrier gas are fed to the spray nozzle whereupon they are atomised into a shower of fine droplets. Thermal energy from the substrate causes a pyrolytic reaction on the sample surface producing crystallites. Any remaining volatile gas is exhausted from the system. Post deposition sintering is required to aid recrystallisation of the deposited film.

The solution compositions can be quite complex and the use of additional toxic chemicals is generally required (in addition to Cd etc.). An example of this is a solution for cadmium sulphide that uses cadmium chloride and thiourea, the reaction for which is given by,

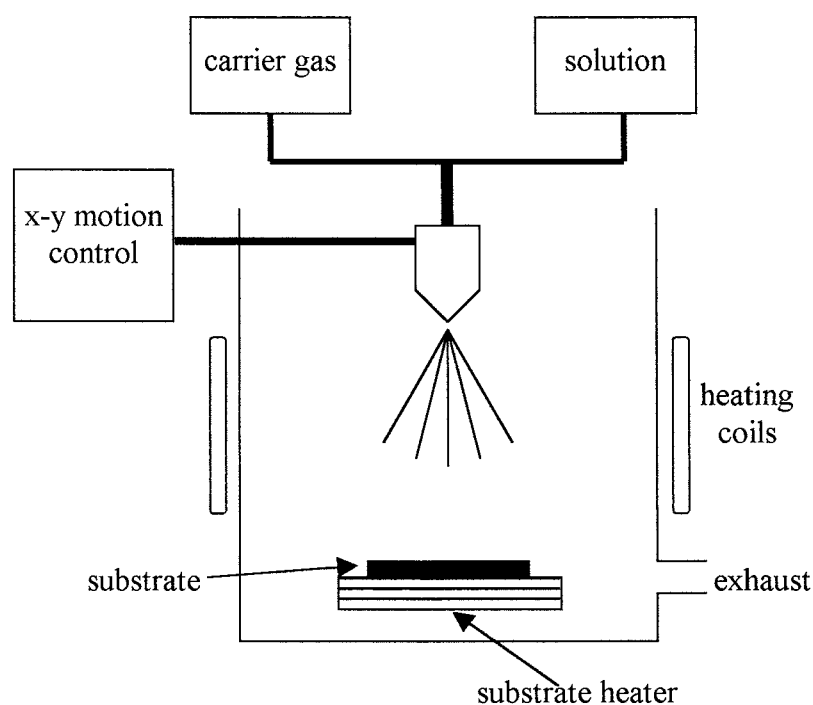
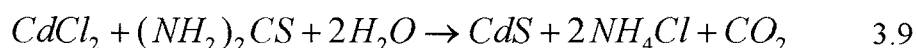


Figure 3.6. Schematic Diagram of Spray Pyrolysis Apparatus.

3.1.8 Thermal Evaporation

To evaporate a source material, enough heat must be applied to the evaporant to reach its vapour pressure. In a vacuum, this temperature is greatly reduced. The Langmuir-Dushman kinetic theory [4] gives the rate of evaporation at a pressure torr,

$$N_e = \frac{3.513 \times 10^{22} P_e}{(MT)^{1/2}} \quad 3.10$$

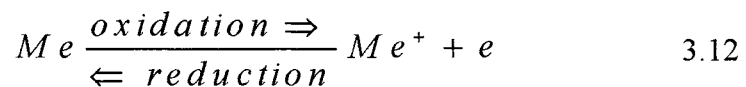
where, N_e has units of molecules $\text{cm}^{-2}\text{s}^{-1}$, P_e is the vapour pressure, T the temperature and M the molecular weight of the vapour. The vapour leaving the evaporant condenses on the substrate, its growth rate being a function of the source-substrate distance. The probability of residual gas molecules in the vacuum colliding with the vaporised evaporant has the exponential function

$$\exp^{(-d/\lambda)} \quad 3.11$$

where, d is the distance between the source and substrate and λ is the mean free path. Typical mean free path lengths are 0.005, 0.05 and 0.5m for vacuum pressure of 10^{-2} , 10^{-3} and 10^{-4} torr respectfully.

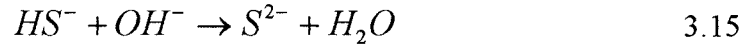
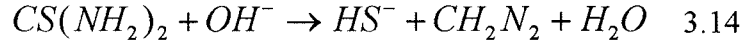
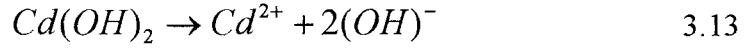
3.1.9 Chemical Bath Deposition (CBD)

Chemical bath deposition (or electroless deposition) is commonly used for the deposition of CdS window layers. As many metal salts are soluble in water, growth relies on a chemical reduction process to aid deposition,



Chemical bath deposition allows control of precipitation in an aqueous solution of metal ions such as Cd^{2+} or Se^{2+} , using a source of ions as precipitating agents. For

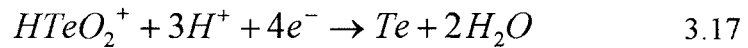
example, S^{2-} or Se^{2-} for CdS and ZnSe films respectively. The precipitating agents are provided by the slow hydrolysis of precursors such as thioacetamide (CH_3CSNH_2) or thiourea ($CS[NH_2]_2$). A typical reaction sequence for CdS is given by,



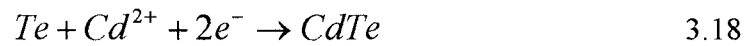
where the dissociation of $Cd(OH)_2$ is the source of Cd^{2+} ions and the decomposition of thiourea produces the S^{2-} ions [5]. When the concentration of cadmium and sulphur ions in the solution exceeds the solubility product of CdS, the formation of an insoluble layer occurs. The temperature and pH of the solution affect ion production, which in turn influences the film growth rate.

3.1.10 Electrodeposition

Electrodeposited CdTe films are grown from an aqueous solution containing a high concentration of Cd^{2+} ions and a low concentration of $HTeO_2^+$ ions. Two steps are required for the deposition of say CdTe, firstly the reduction of tellurium,



and a rapid reaction with the Cd^{2+} ions in the electrolyte



However, if the above reaction is too slow then a Te rich film is formed [6]. Because TeO_2 has low solubility, the concentration of $HTeO_2^+$ is proportional to the current density and the rate of agitation (mechanical stirring), leading to a low deposition rate. However, this allows good coverage and uniformity of coatings on substrates with large areas.

3.2 II-VI Binary and Ternary Alloys

When considering chalcogenide systems, there are six binary alloys of interest which are based on zinc or cadmium cations (metal atoms) and sulphur, selenium or tellurium anions (non-metal atoms). The variation of energy bandgaps as a function of lattice constants for the constituent binary components are shown in figure 3.7.

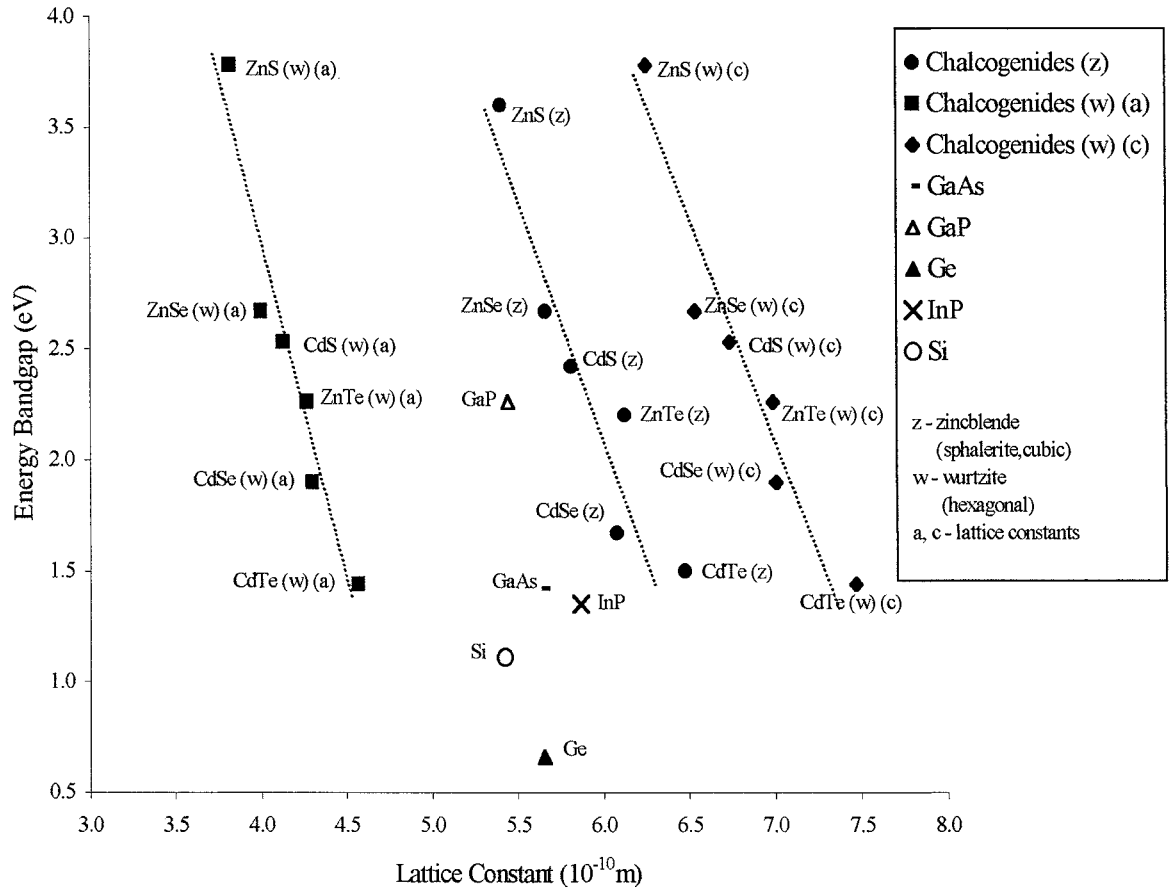


Figure 3.7. Energy Bandgap as a Function of Lattice Constant for Zn or Cd Cations and S, Se or Te Anions with Other Possible Heterojunction Partner Semiconductors.

One of the main considerations when forming a heterojunction between systems is lattice matching. That is the joining of, say two binary systems with the same lattice constants. However, most bulk chalcogenide binary systems are metastable in either sphalerite or wurtzite structures. Yeh et. al. [7] investigated the energy difference between these two systems as a function of binary anions, as shown in figure 3.8. These data show that positive $E_{(w)} - E_{(z)}$ values indicate a preference to

the sphalerite system. However, stable sphalerite systems can be susceptible to twinning, but compounds with low (and negative) stabilisation energies can be affected by planer defects, prone to polytypism and also susceptible to twinning.

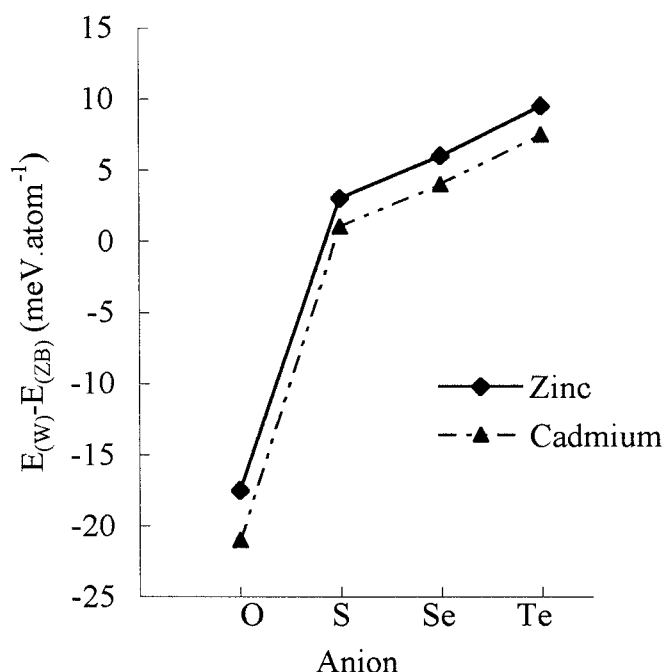


Figure 3.8. Calculated Energy Differences Between Wurtzite and Zincblende Structures at Room Temperature (from [7]).

Another consideration is the systems bonding type. Wurtzite and zincblende structures can both be described using the tetrahedral system. This model is ideal for zincblende (and diamond) structures and nearly perfect for most wurtzite structures [8]. This allows the bond length d to be used to describe the semiconductor properties. For all of the chalcogenides of figure 3.7, the d values of both crystalline systems are almost identical and can therefore be used, in part, when considering lattice matching of binary and possibly ternary systems.

When two sphalerite binary alloy systems AC and BC are mixed, a ternary alloy described by $A_xB_{1-x}C$ is formed. High miscibility of this alloy is possible when A and B have the same valence and both AC and BC belong to the same octet structure (i.e. AC and BC are I-VII, II-VI or III-V alloys). Many of the structural and optical properties of the ternary system can be represented by the relationship between the end binaries (i.e. AC and BC) rather than a whole new alloy system. This leads to

the realisation of a relationship between the end binaries. If F describes a property of the ternary system, and F_{AC} and F_{BC} are the properties of the end-point compounds, then the weighted average of composition x can be given by [9]

$$\overline{F}_{(x)} = xF_{AC} + (1-x)F_{BC} \quad 3.19$$

and can be fitted by the quadratic equation

$$F_{(x)} = \overline{F}_{(x)} + kx(1-x) \quad 3.20$$

where k is a bowing parameter which is independent of the composition and where $F_{(1)} = F_{AC}$, $F_{(0)} = F_{BC}$. Extending this theory leads to an equation for the lattice constant as a function of alloy composition. The lattice constant generally stays close to its concentration average $\overline{a}_{(x)}$ as described by Vegards law and given by [9]

$$a_{(x)} \approx \overline{a}_{(x)} = xa_{AC} + (1-x)a_{BC} \quad 3.21$$

which effectively states that there is a linear relationship between the constituent end binary compounds. Apart from a few materials [10], this is generally the case with most ternary alloy systems. On the contrary, the optical properties in many instances do not follow the linear example of the lattice constants. Again using the general relationship of equation 3.19, the energy bandgap of a ternary system can be described by [9]

$$\overline{Eg}_{(x)} = xEg_{AC} + (1-x)Eg_{BC} \quad 3.22$$

and a quadratic relationship of the form

$$Eg_{(x)} = \overline{Eg}_{(x)} - bx(1-x) \quad 3.23$$

or [11]

$$Eg_{(x)} = Eg_1 + ax + bx^2 \quad 3.24$$

where a and b can be positive or negative and where b is the composition independent optical bowing parameter.

Woolley [12] and others have attempted to find a linear relationship between optical bowing, lattice mismatch ($a_{AC} - a_{BC}$), energy bandgap mismatch ($Eg_{AC} - Eg_{BC}$) and electron affinity mismatch ($\chi_{AC} - \chi_{BC}$), without success. Understanding the relationship between these attributes is paramount to device performance. However, the most important parameter is the energy bandgap, which is generally the first characteristic considered when designing heterojunction devices. Many models have been applied to ternary alloys, the first of which being the virtual crystal

approximation model (VCA) [9]. The VCA model replaces the individual elements, A and B, of the system with an average or virtual element AB. This idea forms the basis of the empirical pseudopotential model (EPM) [13], the dielectric two-band model (D2BM) [14] and the hybrid pseudopotential and tight-binding method (HPT) [8]. Diagram 3.9 shows the calculated bowing parameters for all the possible ternary alloy combinations of ZnSSe / CdTe heterojunctions (bowing data from HPT method used in Chen and Sher [8] and assuming linear lattice constant between end binaries). However, care should be taken when using the data determined using the tight-binding method, as in some cases, agreement between the theoretical and experimental is not found. For example, HPT-ZnSSe = 0.662eV compares favourably with experimental data of section 3.3 and this work (section 5.2.8) and HPT-CdZnSe = 0.266eV and experimental 0.25eV [15]. Whereas, in other cases, two completely different results are obtained, HPT-CdSTe = 0.303eV and experimental 1.74eV [16].

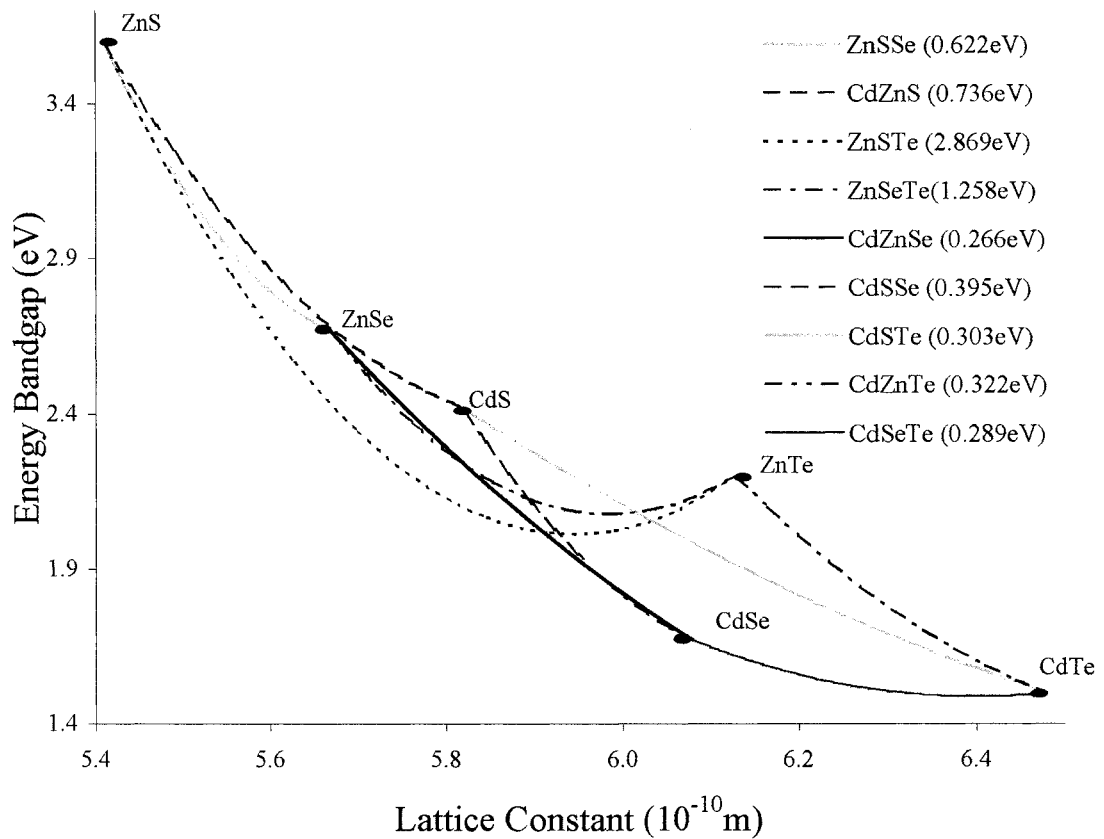


Figure 3.9 Energy Bandgap as a Function of Lattice Constant for Zn and Cd based Chalcogenide Ternary Alloys showing Optical Bowing Parameters.

3.3 ZnS_xSe_{1-x} Ternary Alloys

One of the first investigations into the ternary alloy ZnS_xSe_{1-x} was carried out in 1957 by Larach [17]. To ensure homogeneity, phosphor-grade zinc sulphide and zinc selenide were dry ball-milled for six hours. After transport to silica boats, material crystallisation was achieved by heating to 900°C and then cooling in an ambient of nitrogen. From measurements of diffuse reflection as a function of wavelength, the energy bandgaps of the compounds were extrapolated. Results here showed a linear (persistence type) relationship between energy bandgap and composition.

Six years later, Morehead [18] produced phosphor alloys of ZnSe and ZnS using Cu and Cl doping to determine the activation levels and enable comparison to the end binary series. The alloys were prepared from mixed powders encapsulated in quartz and fired at 950°C for 2.5 hours. After an air quench, the alloys were then washed with cyanide. Measurements of emission, excitation, photoluminescence and electroluminescence were carried out on a range of ZnSSe samples. Results showed a variation in bandgap with alloy composition and therefore a systematic shift in optical properties. When these data were compared with other chalcogenides (i.e. ZnTe, CdTe, CdS and CdSe) with the same cation, (i.e. either Zn or Cd) the separation between the donor level created by the Cl doping and the conduction band was constant. A similar finding was reported for like anions (i.e. S, Se and Te) and energy separation between the acceptor level and valence band caused by Cu doping. This indicated a good agreement with the ionic model of II-VI alloys, which postulates a cation association with the conduction band and the anion with the valence band.

In 1967 Brafman [19] investigated the optically active phonon processes in ZnS_xSe_{1-x}, believing this was the first time that such a thorough treatment had been attempted on a mixed crystal system. Infrared reflection, transmission and Raman spectroscopy of the mixed crystals were used to determine the longitudinal optic (LO) and transverse optic (TO) phonons at $\mathbf{k} \sim 0$. In mixed crystal systems, the interaction between atoms can be of an ionic or covalent nature and one set, or two sets respectively, of long wavelength optical phonons are found. Results showed that that the ZnS_xSe_{1-x} crystals investigated indicated signs of both ionic and covalent systems,

however a linear relationship for the long wavelength optic modes of the mixed crystals was found.

With the intention of producing blue light emitting diodes, in the mid seventies Cutter [20] investigated vapour phase growth of ZnSSe. Vapour growth of ZnSe was by then considered a routine procedure, however the growth of ZnS using the same method was not. ZnSe crystals were grown at a temperature of approximately 1100°C, producing a stable sphalerite structure. ZnS could be grown with the hexagonal phase but required higher temperatures to form in the sphalerite phase. The mixed ZnSSe crystals therefore also have mixed cubic and hexagonal phases. Cutter et. al. set out to investigate whether mixed ZnSe and ZnS crystals can be grown in a single phase using the vapour phase technique. Transmission electron microscopy was used to investigate the crystalline perfection and defect structure of samples cut from ZnSSe boules. Their results showed that vapour phase growth of homogeneous $\text{ZnS}_x\text{Se}_{1-x}$ for x values up to 0.6 could be achieved. Also ZnSe tends to form with covalent bonds and ortho-twins prevail due to relief of thermal stress. However, as the sulphur replaces the selenium, ionic bonds are formed which in turn corresponds to formation of the wurtzite structure and random stacking faults. It is concluded that in mixed material systems, both thinner twins and isolated stacking faults should be anticipated.

Cubic crystals of $\text{ZnS}_x\text{Se}_{1-x}$ grown by iodine vapour transport were characterised using optical reflectometry by Kirschfeld [21]. The alloy composition was determined using x-ray fluorescence to an accuracy of 0.1% mole. Room temperature reflectivity measurements in the energy region 2.5 to 9.5eV were recorded and a Kramers-Kronig analysis was carried out on the data. Kirschfeld et. al. postulated that the results obtained could only be explained using the persistence alloy theory. Also from the observed spectra, the Zn bands were split by a separation energy of 0.3eV, apparently caused by different neighbours of sulphur and selenium. Finally they observed both direct and indirect optical transitions.

In 1974, Ebina [22] again used optical reflectivity measurements to determine the lowest energy gap, its spin-orbit-split gap at room temperature and investigate the prevailing alloy system type. Single crystals of $\text{ZnS}_x\text{Se}_{1-x}$ were grown using a high pressure melting technique, creating a boule 30mm long and a diameter of 15mm. Crystals across the whole composition range were produced. Assuming Vegards law, the composition was determined from lattice constant measurements using X-ray

diffractometry. Results indicated that the energy bandgap (and spin-orbit-split gap) did not vary linearly with alloy composition but showed an amalgamation type structure which was fitted using quadratic equations. The bowing parameter for the energy bandgap was found to be $0.630 \pm 0.030 \text{ eV}$ and was in good agreement with virtual-crystal approximation model of Richardson.

Low [23] reported what appears to be the first polycrystalline $\text{ZnS}_x\text{Se}_{1-x}$ composition in 1976. Using a hot press apparatus, the ZnSe and ZnS powders were mixed and loaded into a graphite die. A pressure of over 10000 psi was applied for thirty minutes at a temperature of 1050°C in an ambient of argon. To improve conductivity, the substrates were then annealed in a $\text{Zn}_{0.95}\text{Al}_{0.5}$ alloy melt at 950°C for 120 hours. Contacts were then made using In – Ga alloys. X-ray diffraction showed that the hot pressed pellets had homogeneous cubic phases and lattice constants that vary with alloy composition. Photoluminescence characterisation of the hot pressed samples found a linear relationship between the emission peaks and the alloy compositions. However, only broad band emission was found for the ZnAl heat-treated specimens. Devices using Au-InGa- $\text{ZnS}_x\text{Se}_{1-x}$ -InGa structure emitted light in the visible region, however the drive current required to produce the same intensity varied with each alloy composition. The best emission intensity for the devices was found with the reverse bias connection (Au negative). The Se rich devices had orange-yellow output, whereas sulphur rich samples had a green-blue emission.

In previous work, Ozsan and Woods [24] had characterised the electroluminescence produced in crystals of $\text{ZnS}_{0.6}\text{Se}_{0.4}$. In 1977 they published work on light-emitting devices prepared across the $\text{ZnS}_x\text{Se}_{1-x}$ composition range [25]. Single crystals grown by the iodine transport technique were used to make the devices. Highly purified powder was placed at one end of an evacuated and sealed silica tube containing iodine. After twelve days of heating in a horizontal furnace at temperatures above 800°C , one centimetre long crystals were formed. All compositions showed the zincblende structure, however their resistivity was high. A further treatment in molten zinc with 10% aluminium reduced the bulk resistivities of ZnSe and ZnS to $1 - 10 \Omega \cdot \text{cm}$ and $10^2 - 10^3 \Omega \cdot \text{cm}$ respectively. Current – voltage measurements were used to test the contacts made to the ZnSSe mixed crystals. Good Ohmic contacts were found using indium on crystals with a sulphur content up to 30%. With 40 to 80% sulphur content, reasonably Ohmic contacts could be achieved

at low voltages (below approximately 0.5volts). However, with high sulphur content, the power law relationship showed n values much greater than 1 (the power law is given by $I \propto V^n$ and Ohmic contacts should have an n value of unity), caused by a thin insulating layer formed under the indium electrode. To obtain electroluminescence from the ZnSSe crystals, two non-Ohmic contacts are required. This was accomplished using gold or indium, depending on the sulphur content of the crystal. In-ZnSSe-Au devices were produced with sulphur molar contents up to 80%. Donor densities of 10^{17}cm^{-3} and 10^{15}cm^{-3} for ZnSe and $\text{ZnS}_{0.8}\text{S}_{0.2}$ respectively were found using capacitance – voltage measurements and the best luminance characteristics were found in devices that operated in reverse bias. For crystals with a sulphur content greater than 80%, devices operating in forward bias produced the highest intensity output in the blue region of the spectrum, with a peak intensity at 470nm.

An interesting paper by Soonckindt [26] investigated energy bandgap as a function of composition and temperature. Bandgap determination was made using an optical technique. $\text{ZnS}_x\text{Se}_{1-x}$ was deposited using vapour phase epitaxy onto CaF_2 substrates. Relying on the Kelvin method, measurement between a reference electrode and contact potential under illumination allows the variation in surface potentials to be obtained. The surface barrier height is directly proportional to the bulk density of free carriers, therefore the bandgap can be found. At room temperature the energy bandgap as a function of composition could be fitted to a quadratic equation and a bowing parameter of 0.63eV was reported. Energy bandgaps as a function of temperature (77 to 300K) across the alloy composition range showed a linear relationship. Polycrystalline samples were also investigated and displayed the same characteristics at room temperature as the monocrystalline structures. However, with temperature dependant measurements, two distinct gradients were observed which were considered to be due to the inhomogeneity of the structure.

Iodine transport was used again by Fujita [27] in 1979 to grow large single crystals of $\text{ZnS}_x\text{Se}_{1-x}$. Prior to sealing in the quartz tube, the powders were baked, mixed and then sintered to clean and purify. X-ray diffraction measurements showed that all powders across the $\text{ZnS}_x\text{Se}_{1-x}$ alloy range had the zincblende crystal structure. These powders were then used as the source material for the iodine transport growth. Afterwards, annealing in molten zinc at 950°C for forty-eight hours improved the

electrical properties of the as-grown crystals. Resistivities of 10^{-2} to $2\Omega\cdot\text{cm}$ and carrier concentrations of 10^{18} to 10^{16}cm^{-3} for $0 \leq x \leq 1$ respectively were displayed.

GaAs and ZnSe are both II-VI compounds having the zincblende crystal structure. However, a lattice mismatch of approximately 0.2% is found between the two alloys. By incorporating sulphur, Scott [28] investigated the possibility of lattice matched $\text{ZnS}_x\text{Se}_{1-x}$ / GaAs heterojunctions. The standard method for epitaxial growth of ZnSe, using elemental zinc and selenium sources with hydrogen flows was modified with the introduction of a sulphur H_2S source. These gases were mixed and allowed to flow over the heated GaAs substrates. Using X-ray diffraction to characterise the layers, lattice matching was found with the $\text{ZnS}_{0.6}\text{Se}_{0.94}$ / GaAs heterojunction.

In 1981, Lewis reported $\text{ZnS}_x\text{Se}_{1-x}$ prepared by chemical vapour deposition (CVD) from zinc vapours and mixtures of hydrogen sulphide and selenide gas [29]. The deposition took place over 150 hours in a reduced pressure at temperatures of 600 to 1050°C . The nature of a CVD system tends to produce high purity crystal. Because non-volatile elements tend to remain in the melt, volatile impurities pass through the deposition system and are exhausted. Energy dispersive spectroscopy (EDS) indicated that the crystals were homogeneous, however some residual inhomogeneity was suggested when analysing the refractive index data. Also, examination of the structural properties of the crystals showed a cubic nature for low sulphur content, but a polytype composition for sulphur rich crystals. Energy bandgap determination from transmittance data was achieved using a quartz-iodine lamp. Photoluminescence and infrared measurements were also used to investigate the emission lines and phonon contributions. Results indicated that by increasing the sulphur content, the emission line could be moved further into the blue region (with some problems of luminescence quenching) and furthermore, phonon processes increase the magnitude of the absorption band.

Lattice matched ZnSSe / GaAs junctions were further investigated by Leigh in 1982 [30]. Again using a hydrogen vapour transport technique, the electrical properties of the $\text{ZnS}_x\text{Se}_{1-x}$ thin films were studied. Schottky barriers were fabricated ($\text{Au}/\text{ZnS}_x\text{Se}_{1-x}/\text{GaAs}/\text{In}$) in order to investigate doping density. Results showed that for x values less than 0.3, the net donor density for the undoped layers was in the range 10^{14} to 10^{16}cm^{-3} . However, the resistivity of the remaining films was greater

than $10^3 \Omega \cdot \text{cm}$ and with sulphur contents above 38%, the layers were semi-insulating. Using capacitance measurements, the built in potentials were extrapolated, with values of 5V obtained for alloy compositions up to 30%. Finally, van der Pauw measurements were carried out on layers with x values less than 0.1, and mobilities of 120 to $108 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ were determined.

The first chemical growth of $\text{ZnS}_x\text{Se}_{1-x}$ in an aqueous solution was reported in 1992 by Chaudhari [31]. Zinc nitrate was used as a source of zinc, thiourea for sulphur and sodium selenosulphate as a source of selenium ions. These three constituents were mixed with sodium hydroxide and water to produce the coating solution. $\text{ZnS}_x\text{Se}_{1-x}$ was deposited onto glass slides and GaAs (110) wafers with the deposition thickness controlled by the solution temperature. Characterisation of the $\text{ZnS}_x\text{Se}_{1-x}$ layers was achieved using XRD, TEM and XRF. Results showed that room temperature deposition produced amorphous layers with a small grain size. However, layers deposited with a bath temperature of 90°C had a polycrystalline nature and a sphalerite structure. Grain growth was also observed at elevated temperatures and lattice matching was achieved with a $\text{ZnS}_{0.056}\text{Se}_{0.944}$ heterojunction

Lattice matching of ZnSSe to GaAs substrates has been extensively investigated. The main drive of this work is for blue light emitting devices such as LED's and lasers. Many reports have suggested that lattice matching occurs with an alloy composition of approximately 6-7%, with most investigations having been undertaken using advanced growth techniques [32,33,34,35]. Lattice matching between $\text{ZnS}_x\text{Se}_{1-x}$ and other substrates has also been investigated. Lee [36] has grown MOVPE $\text{ZnS}_{0.86}\text{Se}_{0.14}$ onto n-GaP substrates, whereas Chen [37] has lattice matched $\text{ZnS}_{0.07}\text{Se}_{0.93}$ / Si heterojunctions and investigated their Schottky diode characteristics.

Reddy [38] has grown ZnSSe by spray pyrolysis using a zinc chloride, thiourea and selenourea aqueous solution. The $\text{ZnS}_{0.5}\text{Se}_{0.5}$ thin films were grown at substrate temperatures of $250\text{-}550^\circ\text{C}$. Substrate temperatures below 350°C produce films with not only ZnSSe, but also secondary phases of ZnS, ZnCl_2 and Se as determined from x-ray diffraction. Thin films grown with temperatures of 475°C were single phase, having the wurtzite crystal structure. Their results show that elevated substrate temperatures are required to necessitate chemical pyrolysis.

The main thrust for investigation into ZnSSe materials has been the need for optical devices that work in the blue region of the spectrum. Jain [39] proposed a

metal-insulator-semiconductor (MIS) structure for efficient blue lasers. The device was modelled using a ZnSe / ZnSSe heterojunction and it was also proposed that both n and p-type doping of the active layer may not be necessary.

Haase et. al. eventually grew the first wide bandgap II-VI laser diode using molecular beam epitaxy (MBE) in 1991 [40]. The light-emitting region of this device was formed around a $\text{Cd}_{0.2}\text{Zn}_{0.8}\text{Se}$ quantum well. A ZnSe cladding surrounded the quantum well, which itself was enclosed in a ZnSSe layer. The device was formed on an n-GaAs, which was lattice matched to the n- $\text{ZnS}_{0.07}\text{Se}_{0.93}$ layer. The layers containing Zn were n-type doped with ZnCl_2 and the p-type layer doped with N_2 . The device was operated at a temperature of 77K and lased at 490nm in the blue-green region of the visible spectrum.

Room temperature ZnSSe quantum well, light-emitting diodes were demonstrated by Xie [41]. Using MBE, the p-ZnSSe layers were lattice matched to p-GaAs substrates. The quantum well consisted of several ZnSSe – ZnCdSe layers with a cap layer of n-ZnSSe. The peak intensity was found to be 494nm, with a maximum power output of 120uW. However, due to the built-in contact barriers, the applied voltage was in the region of 20 volts, which represented an external quantum efficiency of only 0.1%.

In 1995, Heuken [42] discussed the possibilities of blue laser diodes and their potential superior qualities over red III-V junctions. It was claimed that II-VI semiconductors working at shorter wavelengths could, in theory, increase the storage capacity of compact disc players or writable optical storage facilities by a factor of 3-4 over their red laser diode counterparts.

More recently, Kuhnelt [43] has investigated the properties of $\text{ZnS}_x\text{Se}_{1-x}$ for optical waveguides. Calculation of propagation constants and field distributions on multi-layered waveguides could be used to optimise the ternary alloys that make them. Lattice mismatch was said to cause radiation losses and scattering, therefore tuned ternary alloys could be less prone to junction losses than binary systems.

Due to its wide bandgap and potential to operate at shorter wavelengths, ZnSSe has also been considered for ultraviolet detectors. Currently, UV is detected by either silicon p-i-n photodiodes or photomultiplier tubes (PMT). Photodiodes based on silicon have low external quantum efficiency in the UV, while PMT's are fragile,

Ref.	Growth Method	x range	Structure	Substrate	Bowing (eV)	Notes
22	From Melt	0 - 1.0	sphalerite	bulk	0.63 +/- 0.03	Tsub = 500K
45	Hot wall evaporation	0 - 0.9	sphalerite (0 ~ 0.75) wurtzite (~0.75 - 1.0)	glass	0.46 -	
46	Evaporation	0 - 1.0	(assume sphalerite)	quartz	0.545 +/- 0.048	
47	Laser ablation	0 - 1.0	sphalerite	quartz	0.805 +/- 0.133	Tsub = 400°C
48	LPE	0 - 0.99	sphalerite	quartz	0.63 at 4K	Grown from Sb ₂ solutions but Sb not detected in crystal layer.
49	MBE	0 - 0.49	(assume sphalerite)	GaAs	0.61 +/- 0.05 at 300K 0.67 +/- 0.04 at 6K	Growth temp 400°C
50,51	MOCVD	0.12 - 0.96	sphalerite	Si	0.63	Tsub = 250 to 300°C
52	PVD (ZnSe) Plasma activation (S)	0 - 1.0	(assume sphalerite)	glass	0.48	
53	Screen printing	0 - 1.0	wurtzite	glass	-	
54	Sputtering	0.05 - 0.75	sphalerite	glass	0.28 for 263K 0.46 for 233K 0.35 for 203K	Tsub = 203 to 263K
26	VPE	0 - 1.0	sphalerite	CaF ₂	0.63	Tsub = 650 to 780°C
55	Sublimation	0 - 1.0	sphalerite	bulk	0.4 at 4.2K	
Ref.	Calculated Method				Bowing (eV)	Notes
13	EPM				0.6	
14	D2BM				0.14	
8	HPT				0.622	

Table 3.1. Data from ZnS_xSe_{1-x} Layers and Crystals Showing Non-Linear Energy Bandgaps as a Function of Alloy Composition.

expensive and have to operate at high voltages. UV detection is required for many applications, including medical, pollution detection and astronomy. Sou [44] has investigated MBE grown ZnSSe for UV photodiodes. Aluminium was used to n-type dope the ZnSSe which was deposited onto GaP substrates. Their results showed that by tuning the alloy composition and therefore its ability to block visible IR radiation, ZnSSe has good potential as a heterojunction partner in UV photodiodes.

Some reports into $\text{ZnS}_x\text{Se}_{1-x}$ have suggested that the relationship between the bandgaps of the end binaries (i.e. ZnSe and ZnS) and the alloy composition is linear [17, 19, 21]. However, the majority of investigations since the mid seventies have indicated a non-linear relationship between the two end binaries. Another notable aspect is the crystalline / polycrystalline structure of $\text{ZnS}_x\text{Se}_{1-x}$. Again the majority of investigations point to one prominent structural type prevailing. Most reports of $\text{ZnS}_x\text{Se}_{1-x}$ growth indicate a preference to form in the cubic or zincblende structure. Other investigations [20, 29, 45] have shown cubic phases at low sulphur concentrations but hexagonal or polytype structures with high sulphur content. The only investigation to show a wurtzite structure across the whole composition range was reported by Kumar [53], where $\text{ZnS}_x\text{Se}_{1-x}$ was deposited using screen-printing. Table 3.1 shows the zincblende bowing parameters of $\text{ZnS}_x\text{Se}_{1-x}$ crystals and thin films grown by various growth / deposition techniques.

3.4 Cadmium Telluride and Solar Cells

The French Scientist Margottet first synthesised cadmium telluride in 1879 and Jenny and Bube investigated the electronic nature of CdTe single crystals in 1950 [56]. Interest in the potential of CdTe for use in photovoltaics dates back to 1956 when the theoretical optimum efficiency as a function of energy bandgap for various absorbers was produced [57]. This showed that the ideal energy bandgap for a homojunction solar cell is almost equal to that of CdTe.

An important factor in choosing CdTe as a material for solar cells is its ability to be grown both n and p-type. This allowed CdTe based homojunction devices to be fabricated by Vodakov in 1960 [58]. Unfortunately these devices were prone to high surface recombination velocities and surface losses associated with deep junctions, which combined to reduce the overall efficiency. These problems were not overcome until the shallow junction design was optimised by Barbe [59]. This solar cell, tested

under AM1 illumination, produced a cell efficiency of nearly 11%. However, to avoid the surface losses associated with the homojunction structure, CdTe heterojunctions partnered with wide bandgap window materials were developed. Much of the development centred on the n-window / p-CdTe device structure, usually fabricated in the superstrate configuration.

Novel devices incorporating cadmium telluride were developed by Cusano in 1963 [60]. The cadmium telluride film was deposited by a vapour phase technique and n-type doped with iodine. A chemical growth of p-type Cu_2Te was deposited on top of this CdTe layer to form a photovoltaic device. The energy bandgap of CdTe is 1.5eV and of Cu_2Te is 1.04eV, thus giving an optical window of approximately 0.5eV of light that can illuminate the pn junction. However, one major problem of this device configuration was found to be the diffusion of copper from the absorber layer into the n-type CdTe. This, and other problems such as moisture and oxygen, adversely affected cell stability.

To overcome some of the problems incorporated with Cu_2Te based devices, the n-CdS / p-CdTe configuration was considered. Due to its higher electron affinity, cadmium sulphide was considered to be the ideal partner to p-CdTe. By having a larger electron affinity, the CdS / CdTe interface should be less prone to spikes and notches in the conduction band [61]. Also, CdS has an energy bandgap almost 1.0 eV larger than CdTe and therefore has the potential to allow more photons to reach the pn junction. However, lattice mismatch between CdS and CdTe is almost 10%, which was thought to be a major contributor to recombination losses at the junction interface.

The first thin film CdS / CdTe heterojunction solar cell was produced in 1969 [62] with an efficiency of only 1%. A SnO_2 coated glass substrate was covered with a CdS layer and then an undoped CdTe absorber layer was deposited to finish the device. Even though this device had a low efficiency, it proved to be the catalyst for research into CdS / CdTe heterojunctions and efficiencies of 6% were produced in by Bonnet et. al. in 1972 [63]. These cells were produced by depositing CdTe, using close spaced sublimation (CSS) onto CdS coated glass SnO_2 substrates. The cell area of these devices was small, (in the region of millimetres) but this device structure and its corresponding efficiency proved that large lattice mismatch may not necessarily be a major problem with CdS/CdTe heterojunctions.

During the mid seventies, deposition of n-CdS onto single crystal p-CdTe, by spray pyrolysis and vacuum evaporation, produced efficiencies of 6.5 and 7.9% respectively [64,65]. However, high efficiency cells (of around 10% or larger) were not reported until the early eighties. Also during this period, many industrial companies become involved with solar cell research and development. Uda et al. of the Wireless Research Laboratory [66] prepared CdS / CdTe solar cells using screen-printing. Pastes of CdS, Cd+Te, C, Ag+In and Ag were sequentially deposited and heated using a belt driven furnace. Doping of the n-CdS and p-CdTe was assisted by the CdCl₂ flux mixed with the paste prior to deposition (9.1 wt% for CdS and 0.5 wt% for CdTe). The cells were fabricated on 10×10cm² borosilicate glass substrates. The electrical properties of the cells were said to be dependent upon the post deposition sintering temperature. The cells fabricated at higher temperatures produced poor short wavelength spectral responses. The poor quality of the junction was believed to be caused by the formation of a thick layer of CdS_xTe_{1-x} at the semiconductor interface. The best intrinsic cell efficiency was reported to be 9% for a cell sintered at 620°C. In addition, a 48-element 24watt module was constructed using 100cm² cells, giving an overall efficiency of 5%.

Using In₂O₃ coated soda-lime glass substrates, Tyan et al. of the Eastman Kodak Company [67] reported 10.5% efficient CdS / CdTe solar cells. Close spaced sublimation was used to deposit the thin films. The substrate for the CdS layer was heated to 550°C in an ambient of air, at 1.0 torr and with a source temperature of 720°C, whereas, the CdTe layer was deposited using a substrate temperature of 600°C, an air ambient of 1.5 Torr and a source temperature of 660°C. It was believed that by using a partial vacuum, the mass transport of the deposition process could be enhanced. It was also shown that the presence of oxygen in the chamber enhanced the p-type characteristics of the CdTe layer and therefore contributed to more efficient solar cells. Electron beam induced studies (EBIC) of devices without the presence of oxygen showed that the photovoltaic peak was almost 3μm away from the CdS/CdTe junction, which is similar to the buried homojunction CdTe cell. However, with the incorporation of oxygen, this peak coincides with the CdS/CdTe interface and the resulting device had much better photovoltaic characteristics. Also, because the photocurrent collection was mainly confined to the depletion region, it was postulated

that by increasing the diffusion length in CdTe, solar cell efficiencies approaching 16% could be created.

Basol of Monosolar Incorporated of California produced thin film CdS / CdTe solar cells by electrodeposition [68]. Using the superstrate configuration, the nominal layer thickness of the ITO, CdS and CdTe were $\sim 4000\text{\AA}$, $500\text{-}1000\text{\AA}$ and $1\text{-}2\mu\text{m}$ respectively. Efficiencies of 8% were found for small area (0.02cm^2) devices and 7% for device with areas of 4.2cm^2 , using an illumination intensity of 100mWcm^{-2} . The CdTe was deposited directly after the CdS, which was believed to be the reason why high open circuit voltages (0.82V) were obtained. If an etch was introduced between deposition stages, the V_{OC} was reduced. It was also believed that the high short circuit current (21mA.cm^{-2}) was due to the large diffusion length ($0.8\mu\text{m}$) of electrons in the CdTe. It was also thought that the very thin CdS layer allowed more electrons to reach the junction instead of the normal process of absorption below 520nm .

In a continuation of their research into fabrication of solar cells using screen printing, the Matsushita Electrical Industrial Company reported cells with efficiencies approaching 13% in 1984 [69]. During previous investigations it had been found that by reducing the thickness of the CdTe layer, the cell's series resistance could be reduced and therefore the fill factor increased (and hence efficiency). However, a saturation point for the fill factor of 50% was found. By reducing the contact resistance between the electrodes and semiconductor layers, it was thought that an increased fill factor would be found. By incorporating 50 – 100ppm of copper into the back contact it was found that the efficiency of the cells could be increased. The copper containing contact was post-deposition heat-treated at 400°C for 30 minutes in a $\text{N}_2(99\%) / \text{O}_2(1\%)$ atmosphere, increasing the device fill factor to 0.6. With an active area of 0.78cm^2 , the best cell had an efficiency of 12.8%, series resistance of 3.8Ω , diode factor of 2.2, and reverse saturation current of $2.3 \times 10^{-8}\text{A}$.

Close-space vapour transport (CSV) was used to produce $\text{SnO}_2 / \text{CdTe}$ cells by ARCO Solar Incorporated with an active area of 4cm^2 [70]. The deposition and processing steps used to fabricate the cells were chosen in an attempt to produce highly efficient yet low cost devices with a high throughput. Investigations into both tin oxide and cadmium sulphide window layers were undertaken. For both layers, the CdTe was deposited using CSV followed by an air anneal, then a chemical etch before screen printing the graphite-silver back contact. Results showed that for the

SnO₂ / CdS / CdTe device, the blue response of the cell was restricted by the CdS layer ($E_g \sim 510\text{nm}$). Under AM1.5 illumination, an efficiency of 9.5% was reported. Two SnO₂ / CdTe devices were also investigated, the first fabricated using CdTe deposited in 1 atm of He and the second using 1 torr of oxygen. An efficiency of 9.7% was reported for the cell produced in He, and 10.5% for the cell at a reduced pressure.

Electrodeposition of solar cells with efficiencies of 10.6% were reported by Basol 1986 [71]. Earlier reports had discussed CdS / p-CdTe devices with a conversion efficiency of 9% [72], again fabricated using electrodeposition. These devices had high open circuit voltages and short circuit currents but suffered from low fill factor (~ 0.5). High series resistance of the p-CdTe layer and poor Ohmic contacts were believed to be the cause of the low fill factor. To overcome these problems, electrodeposition of a mercury cadmium telluride (cadmium rich) absorber layer was used, forming a CdS/p-Hg_{1-x}Cd_xTe heterojunction [72]. The illuminated characteristics of the best device were $V_{OC} = 0.62\text{V}$, $I_{SC} = 27.03\text{mAcm}^{-2}$, efficiency (η) = 10.6% and an increased fill factor (FF) of 0.63.

Chu et. al. [73] discussed the three criteria for heterojunction partner selection, namely that of electron affinity, thermal expansion coefficient and lattice parameters. It was also pointed out that no ideal partner for CdTe was available but cadmium sulphide and indium tin oxide have been successfully used. CdS / CdTe solar cells were also reported with an efficiency over 10%. Using vacuum evaporation, 0.1–0.2 μm thick CdS layers, with a resistivity of 2-5 Ωcm , were deposited onto tin oxide coated glass using a substrate temperature of 200-250°C and source temperature above 800°C. Before deposition of the CdTe layer, the substrate and CSS plant were “in-situ” cleaned by heating in a reducing atmosphere. The CdTe films were then deposited using CSS. The source-substrate separation was 1mm or less, substrate temperature 500-600°C and the source temperature 600-700°C. The as deposited CdTe layers were found to have high resistivity (10⁴ Ωcm), however, by p-type doping with antimony, their resistivity was reduced to approximately 10³ Ωcm . The p-CdTe was then treated using a potassium based etch before the deposited copper doped graphite back contact was annealed in hydrogen. Device characterisation showed a reverse saturation current of 10⁻⁹ Acm^{-2} (room temperature), a diode factor of 1.6-1.7, fill factor of 0.63, open circuit voltage of 0.75V and a short circuit current of 22.2 mAcm^{-2} , yielding a cell efficiency of 10.5%.

In 1988, Ametek Applied Materials Laboratory reported a novel CdTe based device with a conversion efficiency of 10.4% for 4cm² cells and 9.3% for a module active area of 51cm² [74]. The principle behind Ametek's approach was to exploit the material characteristics of CdTe instead of trying to alter its properties. This culminated in the production of an n-i-p thin film solar cell, the energy band diagram of which is shown in figure 3.10. Three main problems associated with p-CdTe heterojunctions were stated as (i) difficulty in preparing high conductivity films, (ii) low minority carrier lifetimes and (iii) difficulty in making low resistivity contacts. Cu has been, and for test cells is still used as Ohmic contacts to p-CdTe. However, over a short period of time, Cu diffuses into the CdTe layer, poisoning the cell and adversely affecting stability. The three principal factors in using the n-i-p structure are (i) the requirement of high resistivity rectifying contacts to the CdTe layer rather than Ohmic, (ii) intrinsic layer field assisting the collection of charge carriers and (iii) CdS and ZnTe are nominally deposited without doping in n and p-type formats respectively. In addition, the electron affinity and bandgap characteristics of the CdTe / ZnTe interface, predicts a free flow of holes (from CdTe to ZnTe) due to low valence band discontinuity, whereas at the CdS / CdTe interface, no barrier is present that could restrict the flow of electrons (from CdTe to CdS). Barriers do exist however, to stop electrons flowing into the ZnTe and holes to the CdS. It was also pointed out that because both ZnTe and CdS are wide bandgap semiconductors, the solar cell could be constructed to allow light to enter from either side.

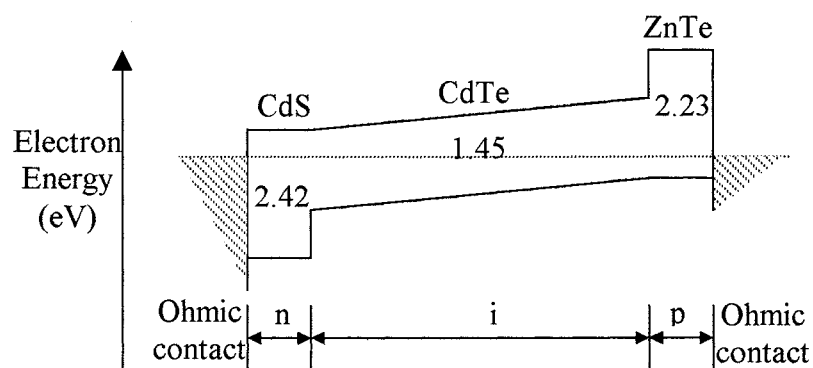


Figure 3.10. Energy Band Diagram of the n-i-p Solar Cell Developed by Ametek [74].

By improving experimental procedures, Suyama of the Matsushita Battery Industrial Company [75] increased the efficiency of screen printed solar cells to

11.3%. One of the major problems with the screen-printed and sintering technique is the cell's strong dependence of collection efficiency with bias voltage. This, and the CdS / CdTe lattice mismatch, adversely affects a cell's photovoltaic properties. A unique feature of this work was the lack of a SnO₂ (or TCO) layer between the CdS and glass substrate. The thick CdS layer was screen printed onto the glass and sintered, then an Ag+In contact was made to it (connected to only part of the CdS layer). The CdTe layer was then screen printed and sintered at temperatures above 600°C. Finally, the CdTe back contact was made using a carbon paste containing a small amount of copper impurities and heated at 450°C for 30 minutes. Improved cell characteristics were obtained by firstly reducing the amount of CdCl₂ (0.05wt%) flux used in the CdS paste prior to deposition and also by increasing the CdS sintering temperature. Secondly, the CdTe sintering ramp up temperature was increased (to 20°C/min) as was the holding temperature (to 660°C). X-ray diffraction and transmission electron microscope (TEM) data demonstrated that by increasing the temperature regimes of both sintering processes, a thin mixed crystal of CdS-CdTe was formed. This interjunction layer is believed to relax the lattice mismatch between the window and absorber layer. Also by improving the CdTe sintering process, EBIC results showed an increase in the minority carrier diffusion length in the CdTe layer. Therefore by reducing the CdCl₂ residue, improving the semiconductor interface and increasing the minority carrier diffusion length, an increased cell efficiency of 11.3% was found for 1.07cm² cells under AM1.5 illumination. .

Using electrodeposition to deposit the CdTe absorber, BP Solar [76] prepared and tested solar modules with efficiencies of over 10%. The idea behind BP Solar's approach was to develop a reproducible, yet safe, fabrication process for CdTe based solar cells. Chemical bath deposition was used to grow the CdS layers on tin oxide coated glass substrates. Electrodeposition was then used to deposit the CdTe in the superstrate configuration. The tin oxide coated substrates were 300mm by 300mm, however substrates up to 1000mm by 600mm were also tested and showed good thickness control and uniformity. Post deposition annealing was used to convert the CdTe p-type, after which the back contacts were deposited. Small area cells (1.0cm²) were used for testing purposes and efficiencies up to 12.7% were reported. A production process was also investigated and showed that out of 100 modules, (300mm × 300mm) the average efficiency was nearly 8%. Nine modules were also

tested in Spain and results indicated that the fractional change in efficiency over a 1600-hour period was less than 3%. The results indicated that CdTe based solar cell modules could be readily produced in such a way that reliability is not a problem.

By optimising the deposition procedures, conversion efficiencies of over 15% were reported by Ferekides et. al. in 1993 [77,78]. The CdS layer was deposited onto fluorine doped tin oxide coated glass using chemical bath deposition. Using CSS, the CdTe layer was deposited with a source-substrate distance of 2 to 6mm in a pressure of 5 to 30 torr. To reduce the effect of light absorption caused by the CdS, the thickness of this window layer was investigated. By reducing the thickness of the CdS from approximately 1150 to 700Å, the spectral response of the cell at shorter wavelengths was found to increase. However, this was to the detriment of open circuit voltage and fill factors which reduced by 20-50mV and 5-10% respectively. Also, by examining the illuminated diode factor it was found that the junction properties appeared to be degrading with decreasing thickness of CdS. By annealing in a H₂ ambient at temperatures up to 450°C, it was found that the energy bandgap of the CdS layer was increased and it was suggested that this could be attributed to grain growth of the window layer. Therefore by combining thin layers of CdS with a post deposition anneal before growing the CdTe layer, the device properties could be enhanced. It was also found that the substrate temperature of CSS deposited CdTe had an important role to play in the photovoltaic properties of the device. By reducing the substrate temperature, the diode factor increased, the CdTe structure changed and the grain size, observed in the scanning electron microscope, got smaller. It was argued that low temperatures were preventing the formation of the mixed crystal Cd_xS_{1-x}Te and in doing so, leaving high concentrations of interface states at the junction. Thus, it was postulated that control of the layers and their junctions was required to achieve high efficiency devices.

A CdS / CdTe superstrate device structure was again used in 1997 to produce a 16% efficient thin film solar cell [79]. Using borosilicate glass, an indium tin oxide layer with a thickness of 200nm was deposited by sputtering. A 50nm CdS layer was then deposited onto the ITO substrate using MOCVD, followed by an air anneal at temperatures up to 400°C. The CdTe was grown using CSS in an ambient of argon and a source-substrate separation of 2mm. Type conversion was achieved using 0.3M of CdCl₂ heated to 420°C for 25 minutes. Finally, screen-printed and sintered carbon and silver contacts completed the device. An important part of the deposition process

was believed to be the anneal between the CdS and CdTe layer depositions. Results indicated that by annealing at 410°C for 10 minutes, the efficiency of the cells was increased. This was achieved by reducing the surface roughness of the CdS layer and hence removing the likelihood of recombination centres around the depletion region. However, over-annealing also had a detrimental effect on cell performance caused by degradation of the indium tin oxide layer. Using ultra thin CdS layers and controlling the fabrication processes were therefore believed to be critical steps in the production of highly efficient CdS / CdTe thin film solar cells.

The highest CdTe efficiency to date was produced by Wu et. al. from NREL in 2001 [80]. Their approach was to replace the SnO₂ with high quality cadmium stannate (Cd₂SnO₄ or CTO) and introduce a high resistivity zinc stannate (Zn₂SnO₄ or ZTO) buffer layer. The cell structure was therefore CTO / ZTO / CdS / CdTe on a glass substrate. The CTO and ZTO were sputtered, the CdS was deposited by chemical bath deposition and the CdTe by CSS. A vapour CdCl₂ treatment at ~415°C for 15 minutes then followed with the addition of Ag paste back contacts. Results indicated a general increase in PV performance with an efficiency of 16.5% reported.

In 1996, Zweibel [81] plotted the progress of high efficiency solar cells as a function of year of manufacture. With the addition of newer data, figure 3.11 shows the development of CdTe based solar cells over the past 25 years. Apart from the work of Matsumoto [69] in 1984, a steady increase in efficiency was found until the early nineties. The jump in efficiencies from approximately 12 to over 15% was mainly due to improved processing and the implementation of the CdCl₂ post-deposition treatment. However, since 1993, little progress in efficiencies has been reported. This is possibly due to the impurity concentrations that exist in the CdTe layer. Durose [82] investigated impurities in close-space sublimation-deposited CdS / CdTe solar cells and found that the impurity concentrations of S, Cl, Cu, Na, and O exceeded the total impurity concentration expected of the CdTe layer before deposition.

Finally, a table containing the reported data from many of the most significant CdTe based solar cells is shown in table 3.2. Compiled in order of efficiency, the striking feature of these data is the small area of the cells tested. To date, larger area modules (4874cm²) have only reported efficiencies of just over 10% [83].

Ref	Layer / Growth Method			area	V _{OC}	I _{sc}	FF	η	Structure	Notes
	(buffer)	(absorber)	(back contact)	(cm ²)	(V)	(mAcm ⁻²)		(%)		
80	CdS / CBD	CdTe / CSS	HgTe:CuTe	1.032	0.85	25.9	0.76	16.5	CTO / ZTO / CdS / CdTe	Used cadmium stannate and zinc stannate
79	CdS / MOCVD	CdTe / CSS	C-Ag / Scr Pr	1.00	0.84	26.08	0.73	16.0	ITO / CdS / CdTe / C+Ag	
77,78	CdS / CBD	CdTe / CSS	C-Hg paste	1.05	0.84	25.10	0.75	15.8	SnO ₂ / CdS / CdTe / C	
84	CdS / CVD	CdTe / CSS	C-Ag / Scr Pr	1.00	0.82	25.41	0.72	15.1	ITO / CdS / CdTe / C+Ag	
69	CdS / Scr Pr	CdTe / Scr Pr	C-Ag / Scr Pr	0.78	0.75	21.80	0.61	12.8	CdS / CdTe / C+Cu/Ag	n = 2.2, I _o = 10 ⁻⁸ Acm ⁻²
76	CdS / CBD	CdTe / ED		1.00	0.81	23.80	0.66	12.7	SnO ₂ / CdS / CdTe	Na = 10 ¹⁵ cm ⁻³ , W _o = 0.54 μm
75	CdS / Scr Pr	CdTe / Scr Pr	C+Cu	1.07	0.80	21.10	0.67	11.3	CdS / CdTe / C+Cu	No TCO used
71	CdS / ED	Hg _{1-x} Cd _x Te / ED	Au/Ni	1.48	0.62	27.03	0.63	10.6	ITO / CdS / Hg _{1-x} Cd _x Te / C+Ag	up to 10% Mercury
73	CdS / VE	CdTe / CSS	C+Cu / paste	1.22	0.75	22.20	0.63	10.5	SnO ₂ / CdS / CdTe / C+Cu	n = 1.6-1.7, I _o = 10 ⁻⁸ Acm ⁻²
70		CdTe / CSVT	C-Ag / Scr Pr	4.00	0.66	28.10	0.56	10.5	SnO ₂ / CdTe / C-Ag	No CdS layer, Na = 10 ¹⁴ cm ⁻³ ,
67	CdS / CSS	CdTe / CSS	Au / VE	0.10	0.75	17.00	0.62	10.5	In ₂ O ₃ / CdS / CdTe / Au	(illumination AM2), n = 1.8, I _o = 10 ⁻¹⁰ Acm ⁻²
74	CdS / Spr Py ZnTe / VE	CdTe / ED	Ni	4.00	0.72	22.30	0.65	10.4	SnO ₂ / CdS / CdTe / ZnTe / Ni	n-i-p device
85	CdS / CBD	CdTe / MOCVD	C-Hg/Cu paste	1.34	0.81	19.60	0.62	9.9	SnO ₂ / CdS / CdTe / C-Hg/Cu	n = 1.7, I _o = 10 ⁻¹⁰ Acm ⁻² , Na = 10 ¹⁴ cm ⁻³
66	CdS / Scr Pr	CdTe / Scr Pr	C+Cu/Ag / Scr Pr	~100	0.71	21.00		9.0	CdS / CdTe / C+Cu/Ag	
68	CdS / ED	CdTe / ED	Au	0.02	0.78	21.00		8.0	ITO / CdS / CdTe / Au	Ln = 0.8 μm

KEY: Chemical bath deposition (CBD)
Chemical vapour deposition (CVD)
Close-space vapour transport (CSVt)

Close spaced deposition (CSS)
Electrodeposition (ED)
Metal oxide chemical vapour deposition (MOCVD)

Screen printing (Scr Pr)
Spray pyrolysis (Spr Py)
Vacuum evaporation (VE)

Table 3.2. Data from Significant Devices Based on CdTe Thin Film Absorber Layers for Solar Cells .

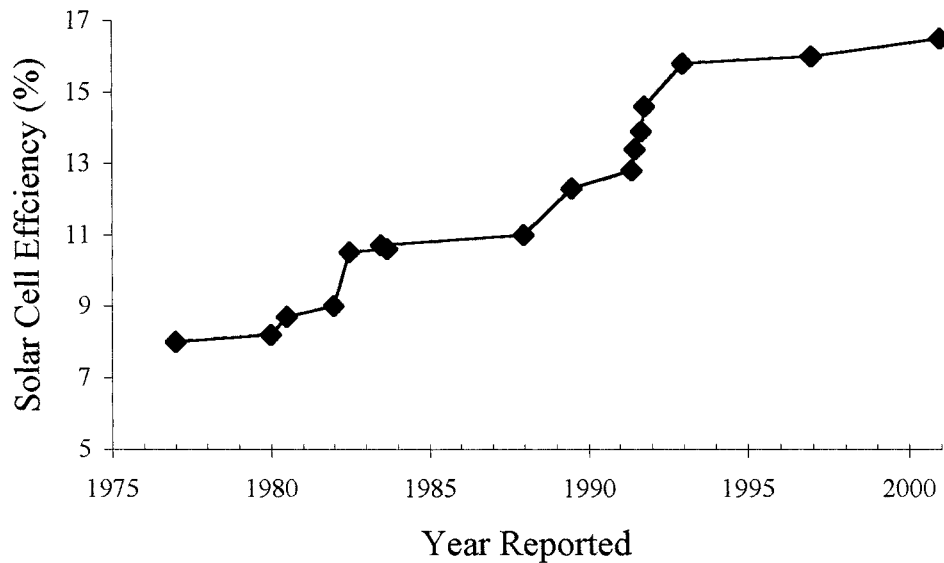


Figure 3.11. Best One-Off Laboratory Solar Cell Efficiencies for Thin Films CdTe (data redrawn from [81] and table 3.2).

3.5 Processing CdTe Based Solar Cells

In section 3.4, the processing steps and development of high efficiency CdTe solar cells was reviewed. Here, the many processing steps required to complete the fabrication of CdTe based solar cells devices are reviewed with reference to their influence on the materials and hence, devices. If, when considering the superstrate approach that has produced the highest efficiencies, then four separate deposition sequences are required, those of the TCO, CdS, CdTe and back contact. Another consideration is the effect that the post-deposition processing and treatments have on the layers and various interfaces, i.e. front contact / TCO, TCO / CdS, CdS / CdTe and CdTe / back contact. A discussion of these processes and post-deposition treatments will now be considered.

An important step in the processing sequence for most efficient CdTe solar cells is the inclusion of a post-deposition treatment. Extrinsic p-type doping of the CdTe is difficult due to the self-compensation mechanisms of the polycrystalline material. Common substitutional dopants for the Te site, for example P, As or Sb, or for Cd substitution, for example group I ions do not work effectively or are difficult to

implement. However, the most efficient solar cells include a CdCl_2 anneal in an oxygen containing environment, which produces changes in the CdTe layer. Two approaches are taken during processing. The first technique is to include the CdCl_2 in the deposition materials of the CdTe layer. This is generally the case when using screen-printing, spray pyrolysis or electrochemical deposition methods. The CdCl_2 is used as a fluxing agent in the mixture and oxygen is incorporated during post-deposition baking, usually in air. The second approach is to include a post-deposition step. The CdCl_2 can be deposited onto the as-grown CdTe by dip coating from solution or vacuum evaporation, followed by an anneal in air. Alternatively, annealing in a chlorine-containing gaseous environment can produce similar results, i.e. Cl_2 , HCl or CdCl_2 vapour.

How the CdCl_2 treatment works is not completely understood, however it has a well-characterised effect on the attributes of the solar cell. The principal role of the CdCl_2 postdeposition treatment is to type convert the CdTe to p-type and enhance junction formation. Basol [86] described what was called the type conversion-junction formation, or TCJF process. The electrodeposited CdTe is typically n-type and has high resistivity but controlling the deposition parameters can produce CdTe layers with p-type conductivity. However, these layers contain excess tellurium and after heat treatment at temperatures above 200°C , the conductivity is reduced due to the evaporation of Te. Therefore, the CdCl_2 treatment is used as a method of obtaining solar grade p-CdTe. The TCJF process was originally developed by the Monosolar group [87]. Using a glass / TCO / CdS substrate, the n-CdTe was formed by electrodeposition. As the CdTe layer already contained CdCl_2 (from the electrodeposition step), the post-deposition treatment only involved an anneal in air for 8 – 12 minutes at 400°C . The TCJF process type-converted the CdTe and formed a rectifying junction between the n-CdS / p-CdTe layers. The Monosolar group also reported a study of the effect the TCJF process on the junction position, as inferred from the spectral response measurements. This was achieved by noting that a buried junction has a long wavelength peak in spectral response, since the long wavelength photons are more weakly absorbed. Conversely, the peak in spectral response is higher at short wavelengths for a shallow junction, since absorption is highest for this wavelength range. Spectral responses and junction positions were reported as a function of the annealing time and temperature. The TCJF process was considered to shift the principal collecting junction from near the CdTe / Au back contact to a

position near the CdS / CdTe junction itself. These changes were revealed by a shift in the spectral response from having a long wavelength peak to having a short wavelength peak, but with improved response at higher wavelengths. It was also shown that the improved spectral response of the cell corresponds to increased fill factor and short circuit current. The Monosolar team believed chlorine and oxygen to be important to the TCJF processing but did not rule out the possibility that residual impurities and interdiffusion (from any of the cell interfaces) might also be a significant variable.

The CdCl₂ treatment is also known to facilitate grain growth, recrystallisation and enhance interdiffusion of the CdS / CdTe junction. An investigation by McCandless [88] set out to examine these effects. Using the superstrate configuration, sequential physical vapour deposition of CdS (0.2 to 0.5 μm at 200°C) and CdTe (0.5 to 4 μm at 250°C) was applied to the glass / TCO substrate. Results for the as-deposited CdS / CdTe indicated single-phase columnar grains for the CdTe film and mixed hexagonal and cubic phase CdS. The CdTe film contained no sulphur (EDS measured) but was highly strained due to the lattice mismatch with CdS. A second batch of CdS / CdTe cells were then post-deposition heat treated at 415°C without CdCl₂. This procedure showed no significant grain growth, yet did promote relaxation of the interface due to interdiffusion of CdS and CdTe. Furthermore, changes to the orientation of the polycrystalline structure were also observed. The final batch, which was heat treated with CdCl₂ at 415°C, indicated significant grain growth of not only the CdTe but also the CdS layer. Moreover, randomisation of the CdTe layer orientation and substantial CdS / CdTe interdiffusion was found. Recrystallisation took place in the first 10 minutes of the CdCl₂ anneal, whereas the interdiffusion continued for a further 20 minutes. The interface diffusion produced a CdTe_{0.95}S_{0.5} alloy, consuming the CdS layer: hence a minimum thickness is required to preserve a distinct CdS layer between the TCO and CdTe.

Another investigation by Romeo [89] reported the effects of recrystallisation in CdS / CdTe cells. It was shown that not only does the CdCl₂ treatment affect the device performance, but the CdS structure does also. High vacuum evaporation (HVE) was used to deposit the CdTe onto either chemical bath or HVE deposited CdS on glass / TCO substrates. The as-deposited CdTe had large grains when deposited on CBD CdS but small grains on HVE CdS. The post-deposition CdCl₂ anneal had little

or no effect on the CBD grains but significant grain growth was found on the HVE CdS. Generally it has been observed [90] that small-grained CdTe undergoes grain growth upon CdCl₂ treatment, whereas large-grained material does not. The link between the substrate and deposition methods and grain growth phenomena is purely one of the as-deposited grain sizes. PVD, sputtering and electrodeposition give small grain sizes that undergo significant grain growth, whereas CSS yields larger grains that are generally insensitive to processing.

The interdiffusion of CdS and CdTe has a strong influence on the spectral response of solar cells. Incorporation of CdTe into CdS narrows its bandgap and reduces the spectral response at shorter wavelength, hence truncating the window of light reaching the pn junction [91]. CdS diffusion into CdTe moves the spectral response to shorter wavelengths since it increases the absorber bandgap. Interdiffusion also lowers the diode ideality factor and indicates a reduction of interface states [91].

The CdCl₂ treatment has also been shown to change the dominant current transport mechanism across the junction [92]. Experiments and modelling indicated that the CdCl₂ treatment changes the dominant current transport mechanism from interface recombination/tunnelling to depletion region recombination. This was presumed to be due to a reduction of interface states upon CdCl₂ processing.

The formation of contacts to p-CdTe has proven to be very difficult due the dearth of metals with a greater work function than that of p-type CdTe. This problem produces a Schottky barrier at the p-CdTe / contact interface which is detrimental to the pn junction performance. An equivalent circuit model proposed by Stollwerck [93] simulated this effect with a second diode of opposite polarity to the primary junction. The characteristics of the additional diode in the model include a barrier height of 0.3eV, lack of light sensitivity and potential for a large leakage current. An equivalent circuit of the model is depicted in figure 3.12. The temperature dependence of the back contact barrier height causes a distinct change in the I-V characteristics when the cell temperature is reduced. Decreasing the temperature of the cell causes the forward current density to become limited: this is known as the forward bias roll-off effect.

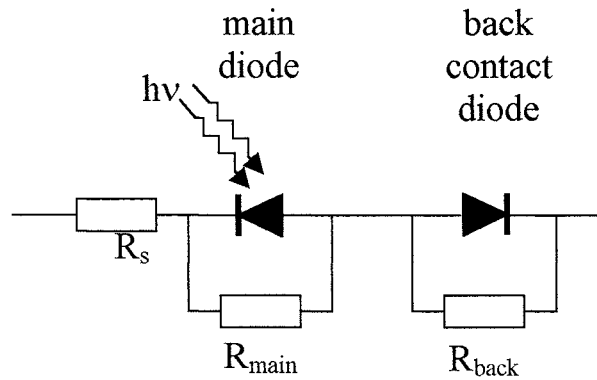


Figure 3.12. Circuit Diagram of Back-Contact Model Proposed by [93].

To overcome the problem of work function compatibility with p-CdTe, three pseudo-Ohmic back contact producing techniques have been implemented.

- (i) Surface doping of the p-CdTe to produce a p^+ layer: This narrows the semiconductor / metal barrier in such a way that charge carriers can tunnel through the barrier.
- (ii) Etching the surface: By altering / controlling p-CdTe surface stoichiometry.
- (iii) Use heterogeneous contacts: Form a heterojunction with another high electron affinity / high conductivity p-type semiconductor that can make near Ohmic metal contacts more readily.

In practice, the most common technique used is to etch the p-CdTe to form a p^+ highly conductive tellurium-rich layer, after which metalisation can be completed. For research purposes, gold and copper doped graphite pastes are the most common contact materials used. However, problems have been found with the tellurium rich surfaces due to the formation of oxides (TeO_2) and an additional reducing agent treatment is often incorporated into the process to eliminate this problem. This phenomenon has been investigated by Chu [94], and oxide formation of the Te and

CdTe underneath the metal contact can lead to a metal-intrinsic-semiconductor structure.

In many cases, a copper or copper-containing compound has been used to form Ohmic back contact to high efficiency solar cells, see table 3.2. It is believed that Cu increases the p-doping of the CdTe near the absorber / back contact interface [95]. However, copper is highly mobile, diffusing through the CdTe layer fairly quickly and therefore degrading the CdTe and CdS / CdTe heterojunction [96].

Romeo et. al. have developed a contact that does not contain any elements that can diffuse into CdTe [97,98]. The Sb_2Te_3 / Mo contacts are highly p-type, have low resistivities and have a forbidden gap of 0.3eV. Cell efficiencies of 15.1% have been reported and light soaking of these cells showed no degradation due to diffusion of back contact elements.

In a study of back contacts, Bätzner [99] investigated the pre-deposition etches and post-deposition annealing requirements for back contact formation. Their results showed that different etchants not only clean the CdTe surface but also produce a Te rich-conducting layer. A nitric-phosphoric acid (NP etch) and Sb/Au back contact produced stable, yet efficient, solar cells. However, the stability of these cells was dependent upon the pre-deposition etchant process.

Another contacting method used autocatalytic deposition of Ni-P alloys [100]. The Te rich surface was obtained using a CH_3COOH etch. Pre-deposition treatments were required to activate the CdTe before the electroless deposition took place. However, this method required post-deposition annealing at temperatures of 250°C to produce a low resistivity contact to the p-CdTe.

Finally, in an interesting experiment using photoelectron spectroscopy, Fritche et. al. developed the energy band diagram for a CdTe solar cell [101]. The whole experiment was conducted within a sealed deposition / characterisation ultra high vacuum chamber. Characterisation of each layer and interface was carried out in order to determine the complete energy band diagram, as shown in figure 3.13. It should be noted that the SnO_2 layer is used to prevent indium diffusion from the ITO layer. Two assumptions were made when forming the band diagram: firstly, that the CdCl_2 treatment strongly dopes the CdS n-type and secondly, there is a p^+ layer forming part of the tunnelling back contact. These two assumptions effectively convert the CdTe into a n-i-p structure, which was said to be in good agreement with results found by other workers.

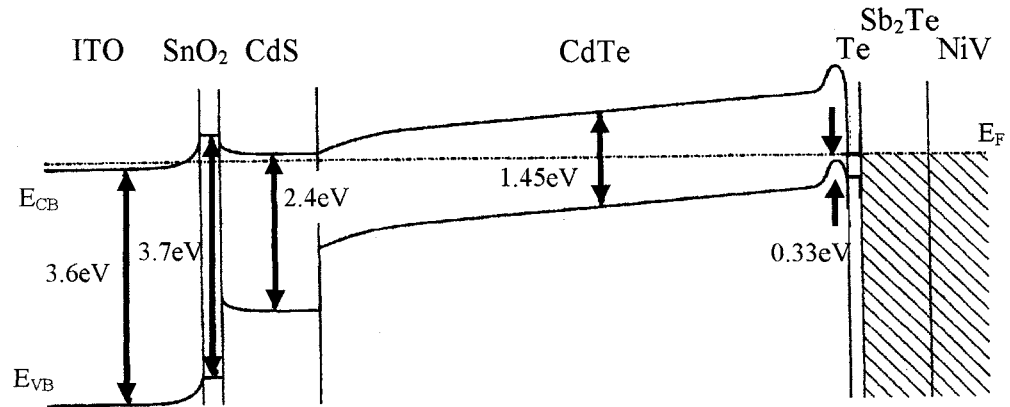


Figure 3.13. Proposed Energy Band Diagram of the CdTe Thin Film Solar Cell [101].

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Chapter Four

Experimental Procedures

4.1 The Deposition System

A schematic diagram of the deposition plant is shown in figure 4.1. A two stage vacuum system is incorporated. The low vacuum (high pressure) stage uses an Edwards rotary vane pump, shown schematically in figure 4.2a. Rotary vane pumps operate by spinning a rotor, which is immersed in oil, inside a cylindrical housing or stator. The oil acts as both a lubricant for the mechanism and a sealing fluid. Spring-loaded vanes move with the rotor and are in contact with the stator wall, forming a seal at all times. During operation, gas molecules enter the chamber and are compressed by the movement of the vane and rotor, thus forcing the discharge valve to open and exhaust the gas to atmosphere. Rotary pumps can generally operate with vacuum pressures less than 10^{-2} mbar [1].

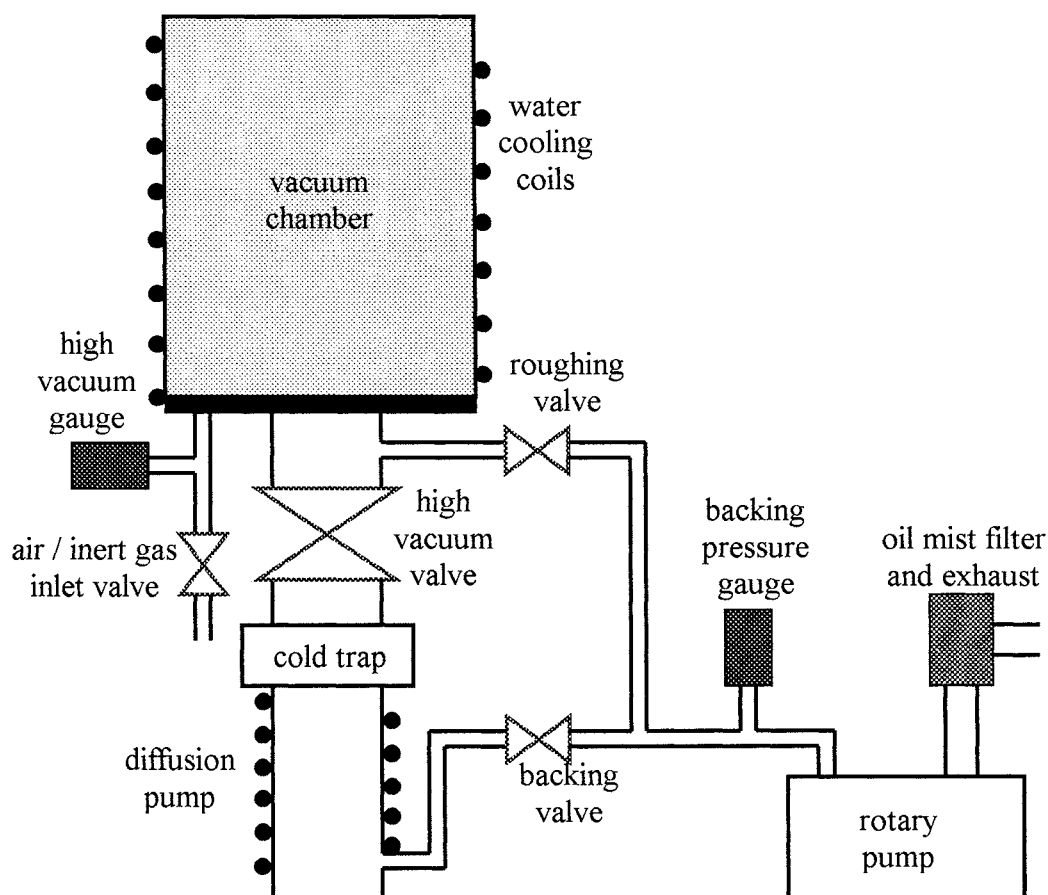


Figure 4.1. Schematic Diagram of the Vacuum Deposition System.

The high vacuum (low pressure) stage uses a Leybold oil diffusion pump, again shown schematically in figure 4.2b. The rotary pump is used to “back” the diffusion pump and ensure that the diffusion chamber pressure stays below 10^{-1} mbar, the maximum working pressure of an oil diffusion pump. The diffusion pump operates by boiling the oil in the base of the chamber using an electrical heater. The resulting hot vapour rises in the chimney and is reflected by the jet cap and nozzles. When a gas molecule is hit by the jet of hot oil, it is forced down to the backing pump and expelled. This process forms an area above the nozzles of reduced pressure. The oil is condensed and recovered by the water-cooling coils around the chamber and hence the cycle restarted.

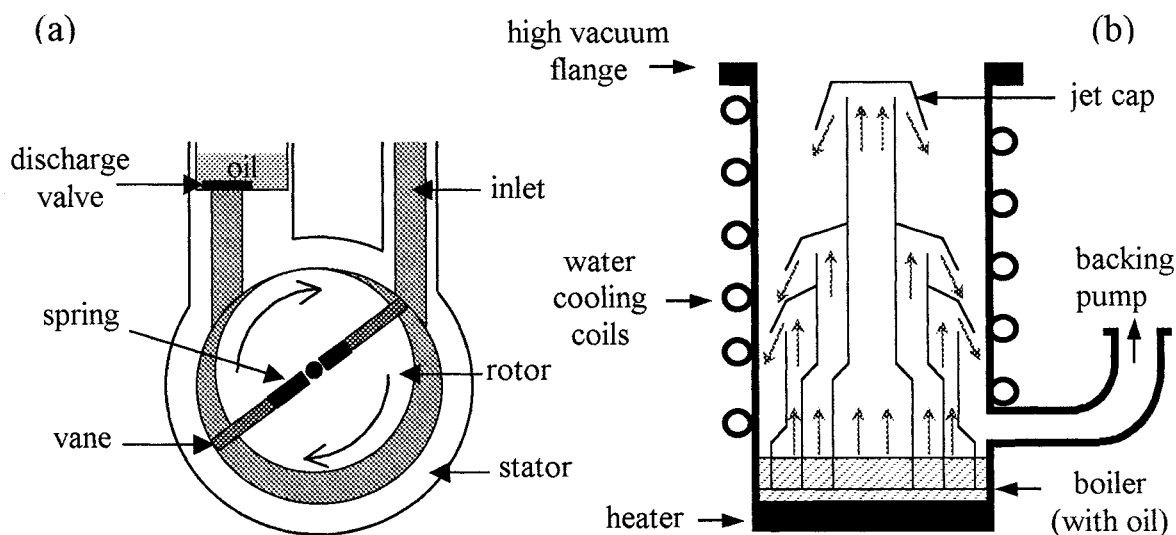


Figure 4.2. Schematic Diagrams of (a) Rotary Vane Pump, (b) Oil Diffusion Pump.

To detect the vacuum pressure, two types of gauges were used. The low or backing pressure is detected using an Edwards Pirani gauge. The Pirani detector measures the rate of heat transfer through the gas as a function of the gas pressure. Measuring the resistance of a heated filament, which forms part of a Wheatstone bridge, achieves this. High vacuum or low pressures were detected using an Edwards Penning gauge. Also known as a cold cathode ionisation gauge, the Penning detector

has two cathodes either side of an anode ring, all of which are surrounded by a magnetic field. A potential difference of 2kV dc is applied between the electrodes, and electrons emitted from the cathode pass through the anode and are repelled by the opposite cathode. Due to this repulsion, and the presence of a magnetic field, electrons form an oscillating field around the anode before eventually being captured by it. Due to collisions between electrons and gas molecules, positive ions are formed and the magnitude of the resulting current produced is proportional to the vacuum pressure [2].

To operate the vacuum system after the chamber is loaded, the roughing valve is opened but only after ensuring the backing and high vacuum valves are closed. The roughing circuit is used to evacuate the chamber and ensure that the diffusion pump is isolated from high pressures (i.e. atmosphere). Once the chamber is below 10^{-1} mbar, the roughing valve is closed and the oil diffusion pump and backing circuit are used to ensure a vacuum below 10^{-5} mbar is maintained within the chamber.

The photograph of figure 4.3 shows the base plate of the vacuum chamber. Three heaters are incorporated within the system, individually controlled by an electrical feedback system shown in the block diagram of figure 4.4. The evaporant was placed in a quartz, bottle-shaped crucible to which quartz wool was added, shown schematically in figure 4.5. The crucible was then inserted into a cylindrical tantalum-heating element purchased from the R.D. Mathis Company. In each case the temperature was measured by a thermocouple in direct contact to the source crucible or substrate. A tantalum baffle was positioned between the source and substrate. The quartz wool and baffle were used to reduce the risk of pinhole formation by the ejection of molten lumps of material from the source damaging the growing film. Pre-deposition outgassing of the chamber and heaters was routinely performed to improve the vacuum pressure during evaporation of source materials. A shutter was also incorporated to control the deposition time.

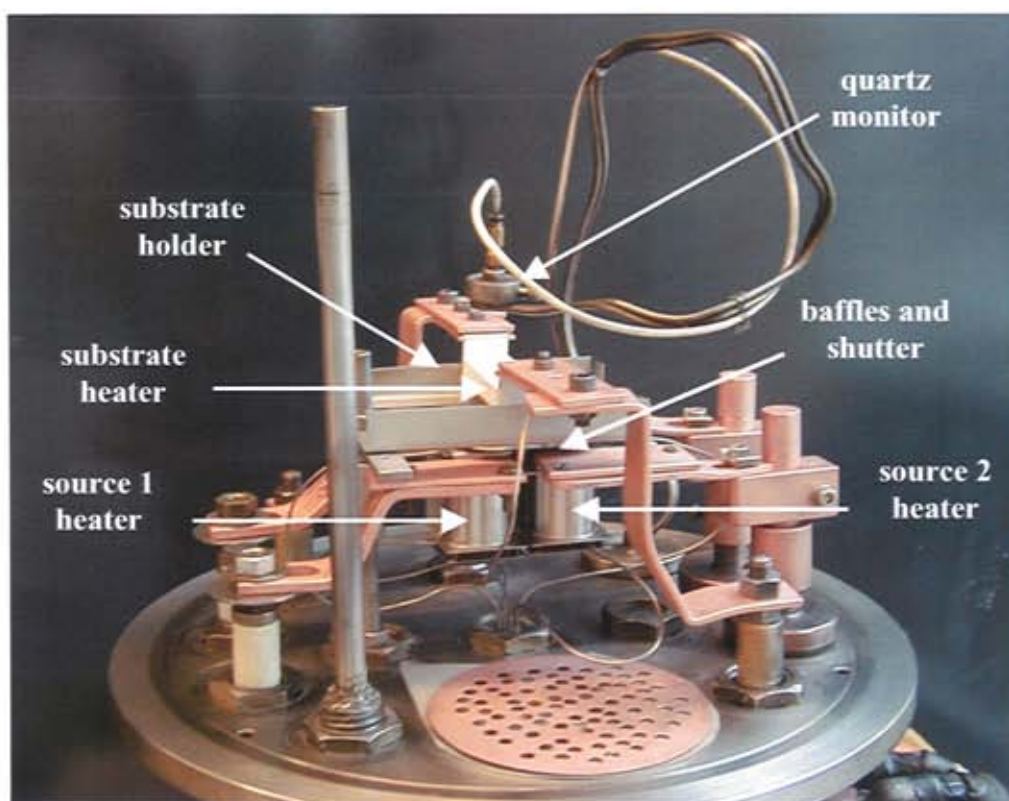


Figure 4.3. Photograph of the Inside of the Vacuum Chamber.

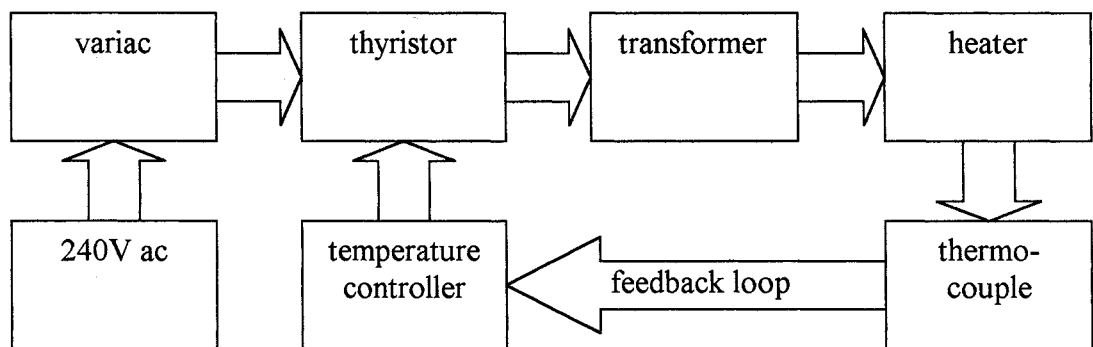


Figure 4.4. Block Diagram of the Electrical System used for Each Heating Circuit.

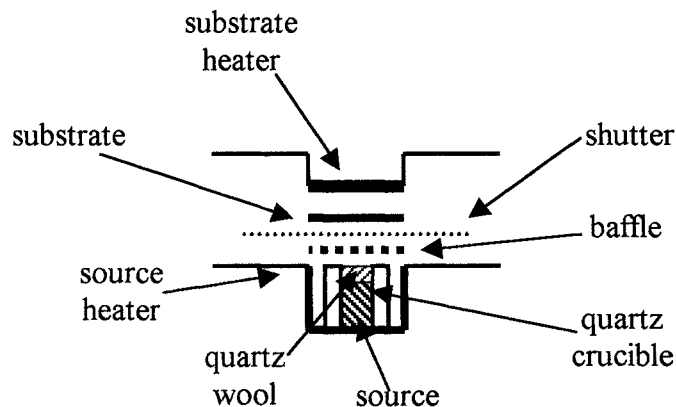


Figure 4.5. Schematic Diagram of the Heaters Showing Source Charging.

4.2 Deposition Processing and Device Fabrication

4.2.1 Pre-Deposition Preparation

The substrates used for deposition were bathed in a cleaning agent (Decon 90) / demineralised water solution in an ultrasonic bath. After a rinse with demineralised water, a further bathe in propan-2-ol (IPA) was used to reflux the substrate in preparation for deposition. On removal from the IPA, the substrates were dried in a stream of nitrogen gas. This process was timed so that the cleaned substrate could be placed directly into the prepared chamber, pre-loaded with deposition materials,

before a final in-situ “dust off” with nitrogen was performed. The bell jar of the plant was immediately replaced and the chamber pumped down using the two vacuum pumps.

4.2.2 CdCl₂ Heat Treatment

An important processing step in the formation of a solar cell containing CdTe is the inclusion of the cadmium chloride heat treatment. The CdCl₂ in powder form was mixed with methanol (CH₃OH) until a saturated solution was produced. Further dilution using methanol allowed the required concentration to be obtained. The coated element was dipped into the diluted CdCl₂/CH₃OH solution for up to five minutes, depending upon the concentration used. After removal from the solution, the CdTe layer was allowed to dry naturally in air before being placed into a furnace. The furnace temperature range used was 350 to 500°C for periods of 10 to 30 minutes. After a further period of cooling, the treated sample was washed in methanol, then finally washed with demineralised water.

4.2.3 Fabrication of Device Contacts

An Ohmic contact to the CdTe was formed using evaporated gold (Au). However, the first step in this process was to prepare the CdTe using a surface etch in the form of a bromine (Br₂) and methanol solution. After etching, the sample was then rinsed using methanol and demineralised water. A metalisation plant was used to deposit the gold contacts. This two stage vacuum plant was very similar in set-up to the deposition plant described in section 4.1. Gold wire was placed onto a molybdenum boat and the sample to be contacted was placed upside down above the wire. The metalisation plant was then pumped down and when the required vacuum pressure was obtained, the molybdenum boat was slowly heated allowing the gold to be evaporated onto the sample. Visual inspection of this process was possible through the glass bell jar of the metalisation plant. To mechanically protect and improve the electrical properties of the Au contacts, a further processing step involved applying a layer of silver DAG, a highly conductive paste purchased from Agar Scientific.

4.3 Characterisation Techniques

4.3.1 Structural Measurements

4.3.1.1 Scanning Electron Microscopy and Energy Dispersive Spectroscopy

A schematic diagram of the scanning electron microscope (SEM) is shown in figure 4.6. The electron microscope used in these studies was an Hitachi S-2400. Electrons are released from the tungsten filament of the electron gun, or cathode, and accelerated to the sample by a field produced by the anode. The fine column of electrons are focused by a number of lenses and apertures and moved across the sample using a raster scan technique. A detector placed near the sample collects a proportion of the photons or electrons displaced from the surface. This signal is then amplified and combined with the scan generator to produce a “picture” of the specimen [3].

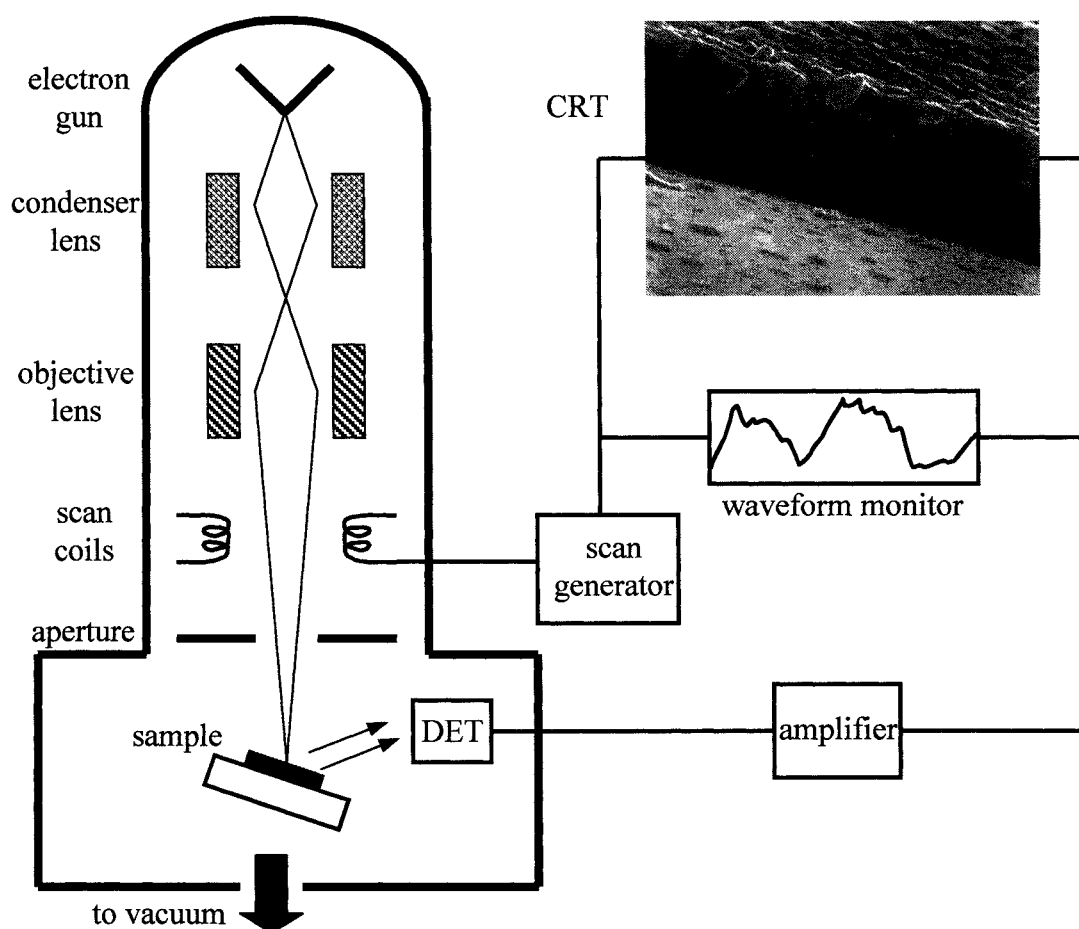


Figure 4.6. Schematic Diagram of a Scanning Electron Microscope (SEM).

There are three principal images produced by the SEM, secondary electron images, backscatter images and elemental X-rays. A diagram showing the source of each radiation is shown in figure 4.7. Secondary electrons are formed by high-energy primary electron interaction with atoms. If an inelastic collision occurs and energy is transferred, then providing this energy is greater than the work function of the material under investigation, a secondary electron is emitted. Secondary electrons have energies less than approximately 50eV and because of their low energy, electrons can only escape from a specimen depth of about 10nm. Backscatter electrons are emitted with energies comparable to that of the primary beam. Like secondary electrons, backscattered images can show specimen topography. However, backscattered electrons can also show atomic number contrast. When the beam passes from low atomic numbers to high, the intensity of the image increases. This is because high atomic number atoms tend to produce backscattering more easily than low atomic numbers.

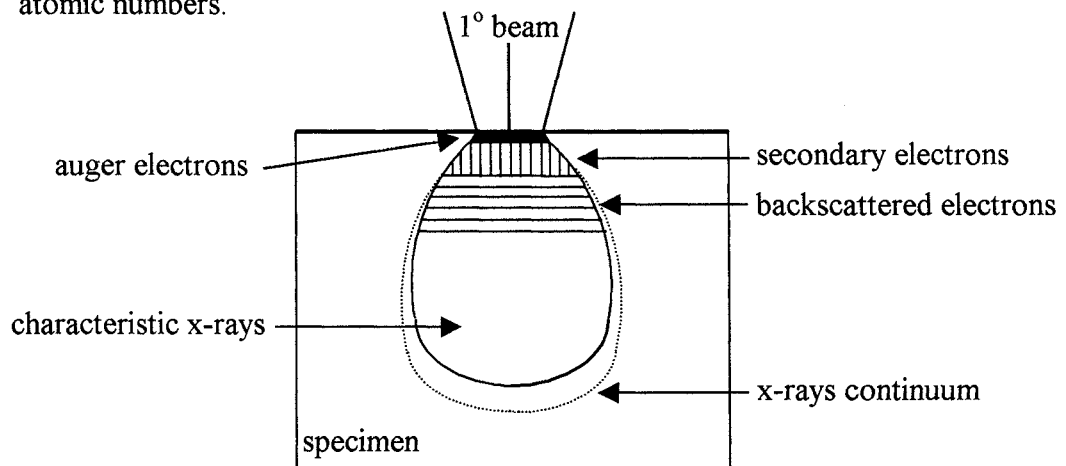


Figure 4.7. Diagram Showing the Origin of SEM Radiation Sources.

In addition to the secondary and backscatter detectors is the energy dispersive X-ray detector (EDS, EDX or sometimes EDXS). When the primary beam ejects a core electron from an atom, the subsequent decay produces a characteristic X-ray photon. The EDS detector can then be used to sort this signal and produce an EDS image or spectrum showing the elemental distribution across the specimen. However, the main problem with EDS is the spatial resolution. This is increased because the primary electrons can travel quite far into the specimen and still have enough energy to produce X-ray emissions. This limits the spatial resolution of the most EDS systems to 0.5 μ m at best [4].

4.3.1.2 Atomic Force Microscopy

An atomic force microscope was used to investigate the topography of the deposited buffer layers. The highest usable magnification available with many SEM's is approximately 80K. This gives a visible region for analysis of approximately $2\mu\text{m}$ by $2\mu\text{m}$. However, the AFM has a resolution of approximately 1nm and can therefore be used to examine specimen areas much smaller than available with the SEM. The AFM uses van der Waals forces to sustain a gap between the atoms of the specimen and the measurement tip. The tip, attached to a cantilever arrangement, deflects a laser beam to a photodetector array. This signal is then amplified and combined with the scanning position from the piezoelectric transducer to form an image in three dimensions. The AFM does not require a conducting substrate, unlike the SEM, therefore insulators or poor semiconductors do not require a conductive coating. The schematic of figure 4.8 shows the basic components of an atomic force microscope [5].

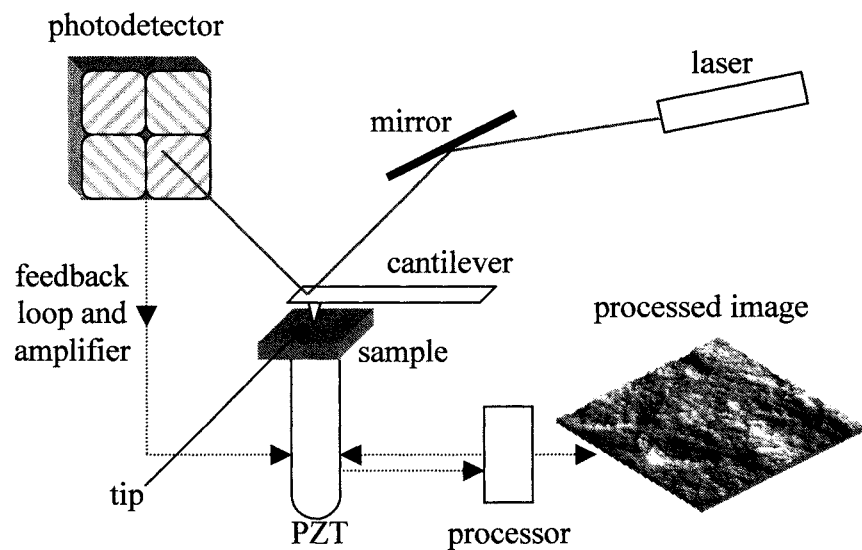


Figure 4.8. Schematic Diagram of an Atomic Force Microscope (AFM)

4.3.1.3 X-ray Diffractometry

The X-ray diffractometer (XRD) is a non-destructive analytical instrument that can determine the crystalline/polycrystalline phases of materials, but specifically in this case, thin film coatings. Structural properties such as strain, phase composition, defects, or grain size can also be determined. The instrument used to determine these properties is a Siemens D5000 X-Ray diffractometer, with a Cu K α radiation source of wavelength 1.5406Å. The specimen in question is irradiated by collimated X-rays, which are reflected from the atoms of the crystallite, see figure 4.9. A diffraction pattern of constructive interference as a function of diffraction angle is produced. The technique is based upon Bragg's law of diffraction given by [6,7]

$$n\lambda = 2d\sin\theta \quad 4.1.$$

where n is an integer, λ is the radiation wavelength, d the inter planar spacing and θ the angle between the incident and diffracted X-rays. An automated system using a PC collects the data. These data can then be used in conjunction with the powder diffraction file (pdf release 1998, data sets 1 – 48 plus 70 – 85), from the International Centre for Diffraction Data, to determine the crystalline phases and their composition.

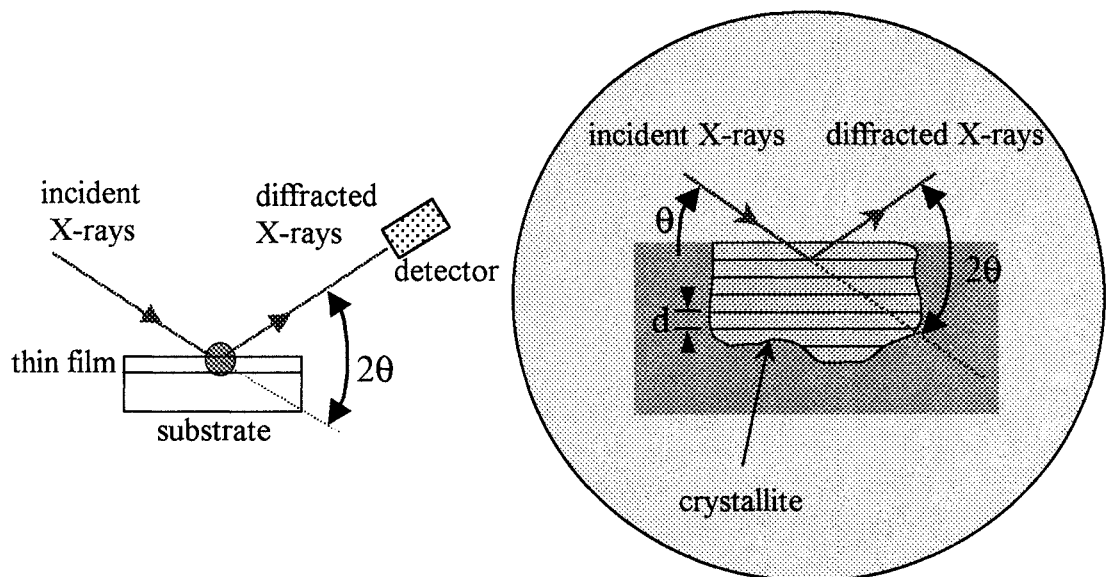


Figure 4.9. Schematic Diagrams of X-Ray Diffraction.

To identify the many d-spacings that can be obtained with constructive interference, a coordinate system of notation for the planes within a crystal is used. These Miller indices have unit vectors a , b and c which form the edges of a unit cell.

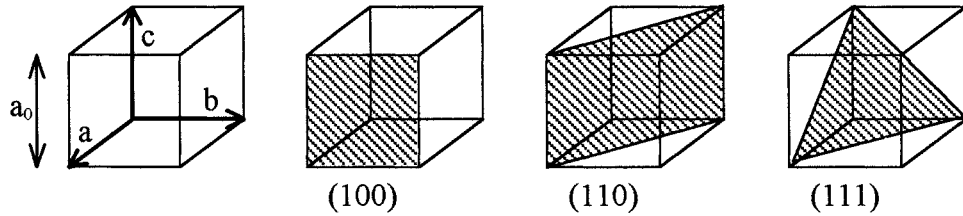


Figure 4.10. Unit Cell and Some Important Indices of the Simple Cubic Structure.

Figure 4.10 shows the unit cell, the lattice constant (a) and some important Miller indices of the simple cubic crystalline structure. To determine the indices, the intercepts on the three axes are found and the reciprocals of each are reduced to their smallest integer. These integers are enclosed in parentheses (hkl) to give the corresponding Miller indices. Incorporating Miller indices allows the Bragg diffraction equation for constructive interference to be written in its correct form (note $n = 1$ for XRD)

$$\lambda = 2d_{hkl}\sin\theta_{hkl} \quad 4.2.$$

The d-spacing between the hkl planes for the cubic (sphalerite) crystalline system is given by

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}} \quad 4.3.$$

and for the hexagonal (wurtzite) system as

$$\frac{1}{d^2} = \frac{4}{3} \left(\frac{h^2 + hk + k^2}{a^2} \right) + \frac{l^2}{c^2} \quad 4.4.$$

4.3.2 Optical Measurements

4.3.2.1 Transmittance, Reflectance or Absorptance Measurements

An Hitachi U3000 spectrophotometer was used to measure the optical transmittance (and reflectance or absorptance) as a function of wavelength of the deposited films. The U3000 has an operating range of 190 to 1100nm. To cover these wavelengths, the instrument uses deuterium and tungsten lamps with a switching point of approximately 340nm (set by operator). Additional parameters to be set are the scan speed and resolution. The U3000 uses two light beams for the sample and the reference or background. Before each measurement session the instrument was calibrated, with the final check being a test run without a sample to ensure a flat response at 100% transmittance. The optical arrangement allows the output data to be collected using two approaches. Firstly the absolute transmittance of the object, in this case the actual transmittance of both the coating and the substrate. A second approach is to take a background reading with the substrate in place allowing the transmittance of only the film to be measured. The output data of the instrument was in the form of a spreadsheet, which can then be plotted using Microsoft Excel.

4.3.3 Electrical Measurements

4.3.3.1 Conductivity Type

A simple, albeit destructive, method to determine the conductivity type of a semiconductor sample is the thermal probe technique [8]. When two identical metal probes are connected to a galvanometer and brought into contact with a semiconductor sample, the instrument is in short circuit. However, if heat is applied to one of the probes, the deflection on the galvanometer indicates the conductivity type. If the semiconductor is n-type, then the heat from the probe causes donor atoms to release their extra electrons, increasing the concentration of free electrons near the probe. However, in order to maintain uniform free carrier concentration, these carriers tend to diffuse away from the probe. Since the electrons have a negative charge, a net positive charge is left behind. Therefore, if this probe is connected to the positive terminal of the galvanometer, a positive deflection is observed. A similar argument can be found for the p-type semiconductor with a corresponding negative deflection.

4.3.3.2 Resistivity Measurement

The Four Probe method is a common technique employed for measuring resistivity. A constant current is passed through the outer two of four equally spaced spring probes and the resulting voltage is measured between the inner two probes, as shown in figure 4.11.

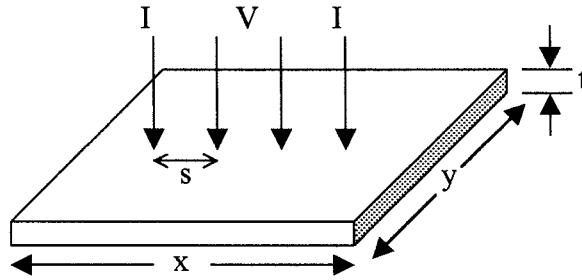


Figure 4.11. Diagram Showing the Four Point Probe Layout.

For the case where the semiconductor is a thin layer the sheet resistance is given by [9]

$$\rho_s = CF \frac{V}{I} \quad 4.5.$$

where CF is a correction factor, however, when the distances x and y are much greater than the probe spacing, s , this becomes

$$\rho_s = \frac{\pi}{\ln 2} \frac{V}{I} = 4.532 \frac{V}{I} \quad 4.6.$$

If the thickness of the sample is known, the bulk resistivity can be determined by

$$\rho = 4.532 \frac{V}{I} t \quad 4.7.$$

4.3.4 Device Measurements

4.3.4.1 Current – Voltage

The current – voltage characteristics of the fabricated junctions and cells were measured using the circuit set-up shown in figure 4.12. By altering the bias voltage of the power supply, the corresponding current was measured. Two Fluke 8010A digital voltage meters with high impedance inputs were used to measure the voltage across the cell and the precision resistor. The voltage across the resistor corresponds to the current flowing through the cell and was converted using Ohms law. Electrical contacts to the cell were made using spring probes to reduce the risk of damage.

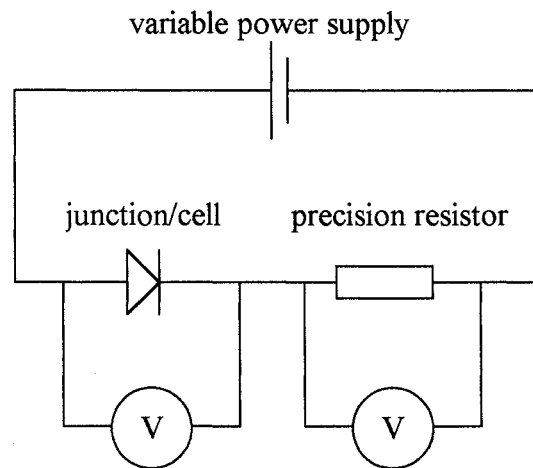


Figure 4.12. Diagram of the Apparatus used to Determine the Current – Voltage Characteristics.

To measure the I-V characteristics under illumination, a 250W xenon lamp was used as a source. Controlled by a stabilised power supply, the intensity of the lamp was calibrated using a pyrometer. The arrangement of the apparatus was adjusted in order to give an intensity of 100mW/cm^2 or 1kW/m^2 , the normalised intensity of the AM1.5 spectrum [10].

The intensity of the light received by the cell could be altered using a set of neutral density filters, allowing new values of V_{oc} and I_{sc} pairs to be determined.

4.3.4.2 Spectral Response and Quantum Efficiency

A diagram showing the optical arrangement used for measuring the spectral response is shown in figure 4.13. A 250W xenon lamp with stabilised power supply was again used as a light source. This radiation was focused onto an Edinburgh Instruments monochromator and the output wavelength was altered using a motor drive. Wavelength calibration was achieved using green (543.5nm) and red (632.8nm) He-Ne lasers. The monochromatic output was measured using a Lasermate-Q system [11] consisting of a silicon photodiode and control unit. The control unit was adjusted to the photodiode response curve, therefore allowing a direct readout of the power at each wavelength set by the monochromator, which is shown in figure 4.14. To measure the spectral response, the photodiode was replaced by the solar cell and the current generated at each wavelength was recorded using the same method as the I-V measurements (section 4.3.4.1).

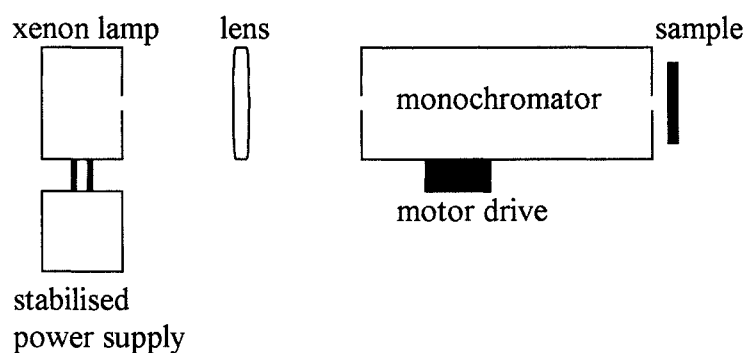


Figure 4.13. Diagram Showing the Optical Arrangement used to Measure the Spectral Response

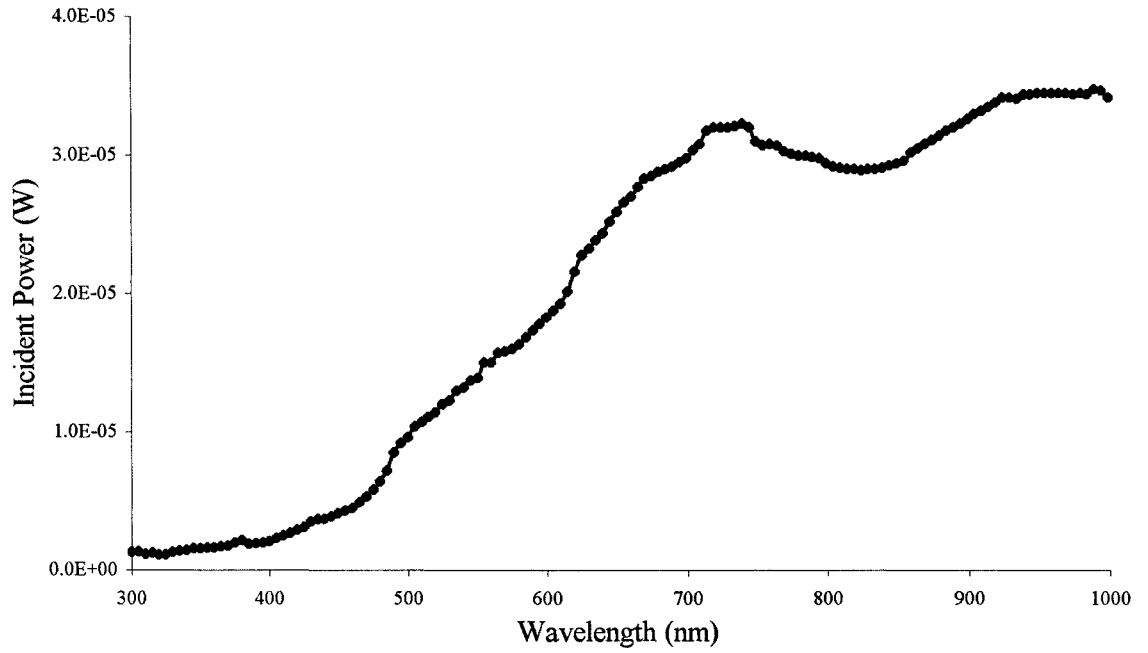


Figure 4.14. Power as a Function of Wavelength
for the Light Source and Monochromator

The spectral response of a cell is the ratio of the photocurrent generated to the power of the incident radiation

$$SR = \frac{I_L}{P_\lambda} = \frac{I_{sc}}{P_\lambda} \quad 4.8.$$

However, the quantum efficiency is defined as the number of photocarriers generated per energy of incident photons at a given wavelength [13],

$$QE = \frac{I_{sc}}{P_\lambda} \frac{hc}{e\lambda} \quad 4.9.$$

In addition, since the area of the photodiode was different from the active area of the device under test, an adjustment was made to compensate, therefore equation 4.9 can be rewritten as

$$QE = \frac{I_{sc}}{P_\lambda} \frac{hc}{e\lambda} \times area \quad 4.10.$$

4.3.4.3 Capacitance - Voltage

The capacitance as a function of voltage was determined using a Hewlett Packard 4274A multi-frequency LCR meter. This instrument allows the voltage and frequency to be selected and the resultant capacitance manually recorded. All C-V measurements were undertaken in the dark and at room temperature.

4.4 References

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Chapter Five

ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ Layers

5.1 Optimisation of Growth Conditions

The deposition method used in these material investigations falls somewhere between thermal evaporation and close-spaced sublimation and has therefore been labelled as close spaced thermal evaporation (CSTE). In conventional vacuum evaporation, material is evaporated by sublimation and condenses on the heated substrate. Typical source - substrate distances $> 20\text{cm}$ are employed. The upper temperature limit of the substrate ($T_{\text{sub}} \sim 400^\circ\text{C}$) is controlled by the rate of re-sublimation and the availability of source material (typical growth rate $\sim 60\text{\AA}\text{min}^{-1}$).

For CSS deposition, the source – substrate distance is typically a few millimetres and takes place in an inert atmosphere. This small distance ensures that a large mean free path is not required for the evaporant to reach the substrate. The geometry of this deposition method allows much higher substrate temperatures and much higher growth rates (up to $10\mu\text{m}\cdot\text{min}^{-1}$ [1]) can be achieved.

The ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers were produced using single source evaporation. The evaporant, with purity of 99.999% purchased from Johnson Matthey, was placed in a bottle shaped quartz crucible. Quartz wool was placed in the top of the crucible which itself was inserted into a tantalum heating element, purchased from R.D. Mathis Company. The quartz wool was used to prevent spattering during deposition, or the ejection of molten lumps from the source, that could potentially damage the growing film. Since the crucible and heater were separate, the purity of evaporant is maintained, as the crucible and wool were replaced each time. For initial testing of the deposition plant and to examine single layers of ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$, the substrates used were soda lime glass microscope slides ($76 \times 26\text{mm}$). These substrates were first washed in an ultrasonic bath containing a degreasing agent (Decon 90) and distilled water for a period of one hour. There then followed a further one hour rinse in distilled water, agitated once again using an ultrasonic bath. Finally the substrate was bathed with propan-2-ol (IPA) to remove any remaining contamination, and reflux the substrate ready for deposition. The cleaned substrate was then placed in the chamber and given a final “dust off” with nitrogen. The metal bell jar was replaced, the cooling water was turned on, and the chamber was pumped down using the rotary and then diffusion vacuum pumps. Once the vacuum pressure was lower than 10^{-5}mbar , which generally took longer than 45

minutes, the source material and substrate were outgassed (with the shutter closed). Typically the source material was heated to $\sim 200^{\circ}\text{C}$ and then allowed to cool, which was found to be enough to outgas the material and crucible but not evaporate the powder. Similarly the substrate was heated to $\sim 100^{\circ}\text{C}$ and again allowed to cool. Deposition did not occur for a further 30 minutes to allow the vacuum to recover. Deposition of the filters took place with an initial vacuum pressure lower than 5×10^{-6} mbar. The source heater was the first to be engaged with a slow temperature gradient, used to ensure a good vacuum pressure was maintained. Once the source temperature approached the set value, the substrate heater was then used to rapidly heat the substrate to the desired temperature. Once both heaters were at their required temperatures, the shutter was opened. During deposition, the vacuum pressure increased but at all times a minimum pressure of 10^{-4} mbar was maintained.

For the layers deposited during these material investigations, the following characterisation assessments were routinely carried out:

- (i) Visual inspection of coating including holding up to strong light source to check for pinholes (not valid for devices due to multilayers).
- (ii) Analysis using SEM to investigate surface topography and grain size / structure.
- (iii) Measurement of optical properties as a function of wavelength to investigate the energy bandgap and absorption characteristics.
- (iv) Measurement of resistivity using the 4-probe method.
- (v) Determination of the structural phases using the X-ray Diffractometer.
- (vi) Measurement of film thickness using the SEM and confirmation by using the interference fringes [2] (where possible).

Initial investigations were carried out with source temperatures of 400°C to 500°C and with substrate temperatures of 200 to 300°C . In most cases, the quality of the coating was poor in terms of adhesion and optical or structural properties. It was concluded that the source temperature was not high enough to ensure the source material was suitably evaporated. However, these problems were overcome by using a source temperature of 600°C

5.2 Characterisation of $\text{ZnS}_x\text{Se}_{1-x}$ Layers

5.2.1 Structure of ZnSe - 25mm / T_{source} 600°C

The deposition plant was set-up with a source substrate distance of 25mm, measured from the top of the heater element to the bottom of the substrate. Figures 5.1a and 5.1b show the microstructure of the coated layers, obtained from the SEM, with varying substrate temperatures and a source temperature of 600°C. Relatively high SEM magnifications are required to resolve the morphology of the coatings, indicating small grains or structure.

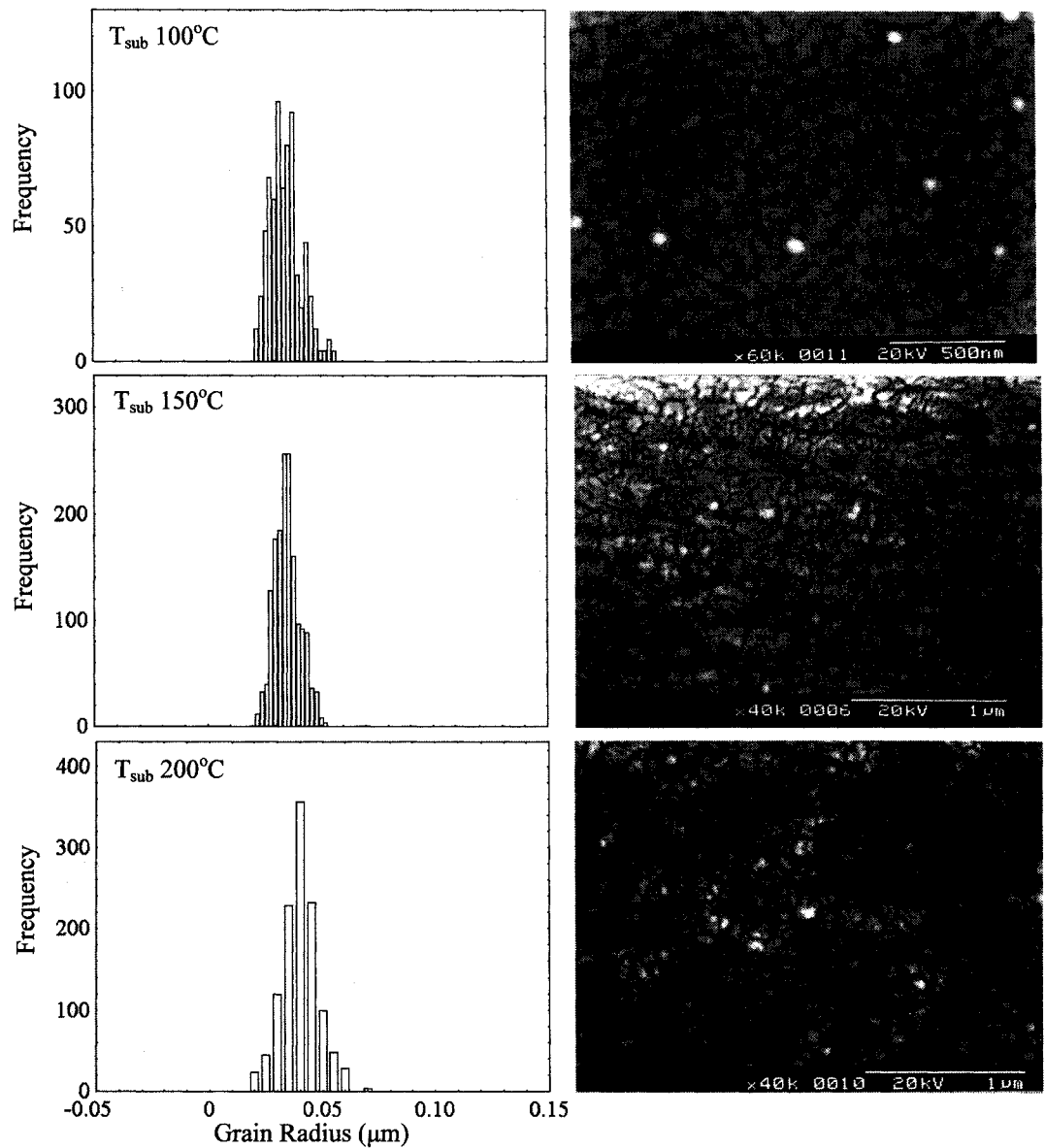


Figure 5.1a. SEM Micrographs of ZnSe Deposited with Parameters 25mm / T_{source} 600°C and Varying Substrate Temperature.

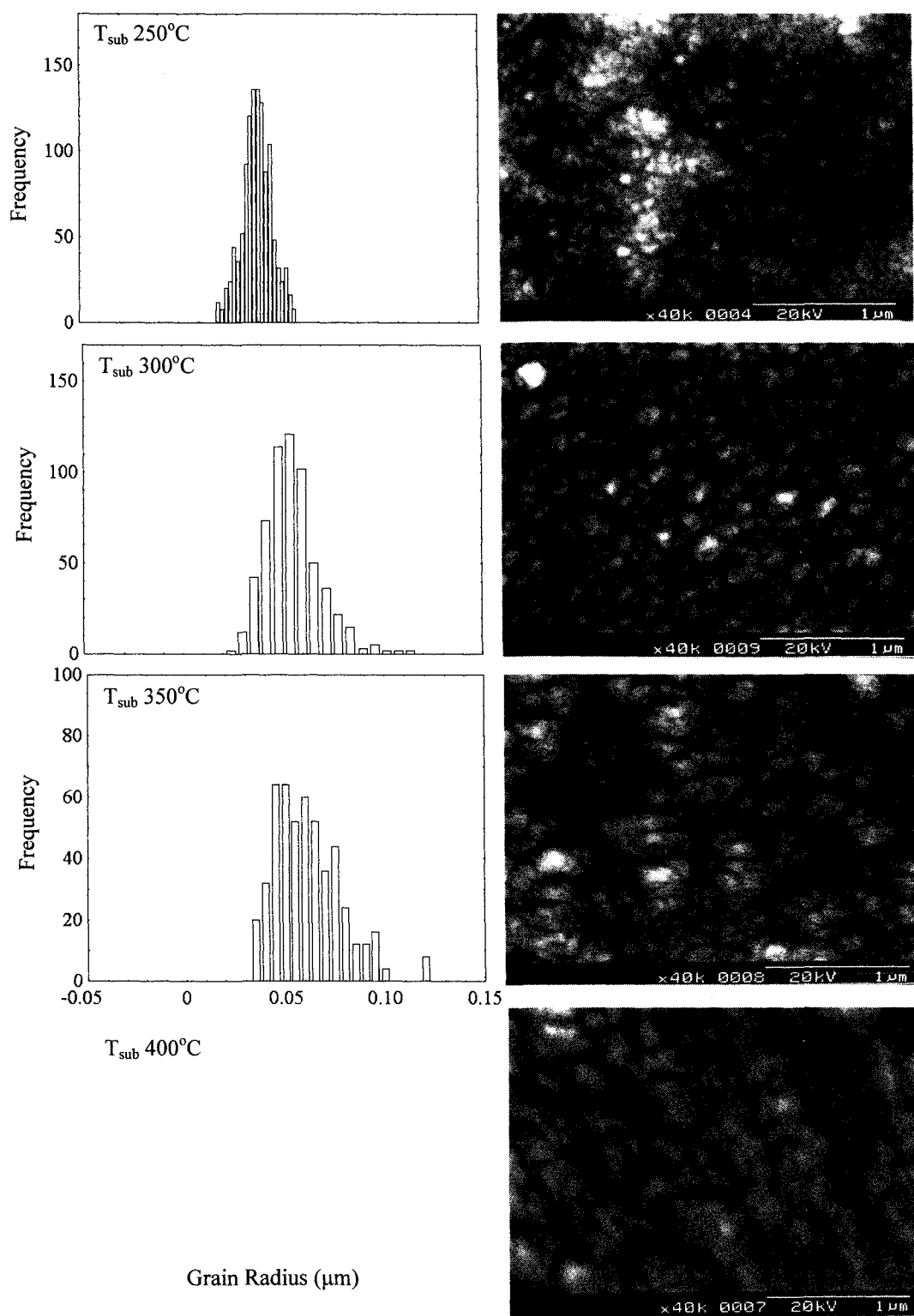


Figure 5.1b. SEM Micrographs of ZnSe Deposited with Parameters 25mm / T_{source} 600°C and Varying Substrate Temperature.

To compare the morphology of the films, the grain structure was studied using analysis software written and developed by [3, 4]. To analyse the grain structure, a developed SEM photograph (20cm by 15cm) was traced and a bitmap image created. This file was then used by the program to create a centroid distribution map of the grains, which is then converted into the histograms shown in figures 5.1a and 5.1b. Figure 5.2 shows a plot of the average grain radius data, taken from the histograms, as a function of substrate temperature. The error in this value was taken from the mean of the average grain radius deviation and the line fit using linear regression. The apparent increase in grain size, with increasing substrate temperature, observed in the SEM micrographs, is confirmed by the data in figure 5.2.

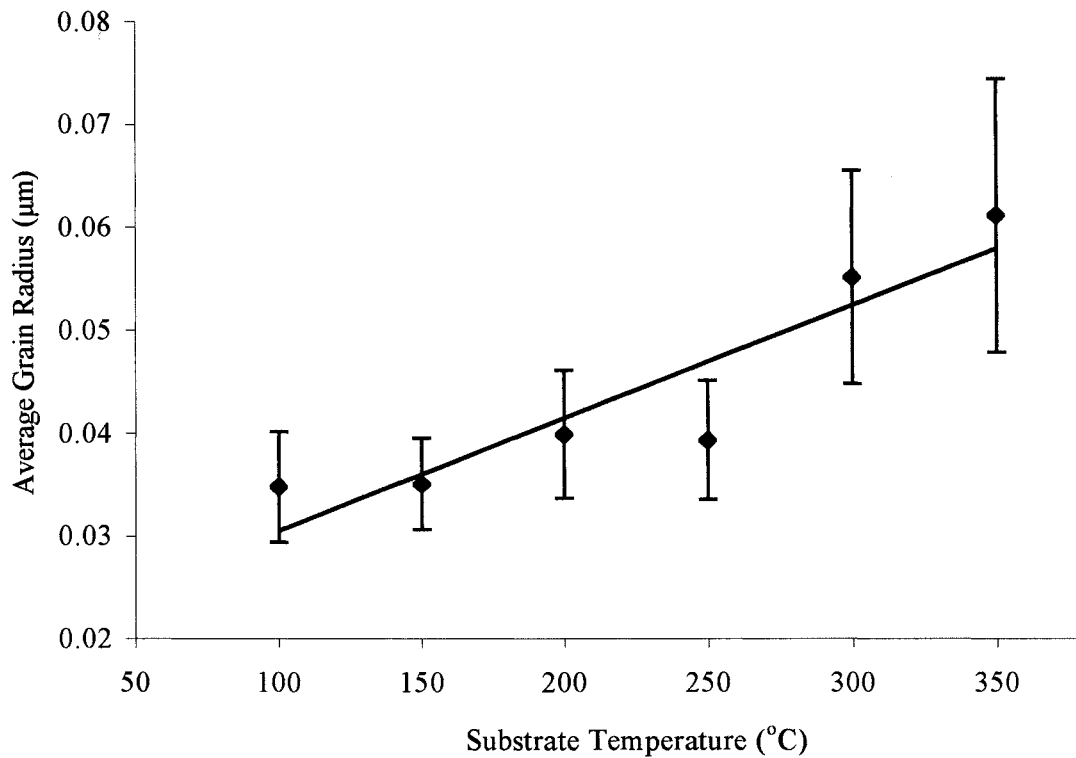


Figure 5.2. Average Grain Radius Versus Substrate Temperature for ZnSe Deposited with Parameters 25mm / T_{source} 600°C.

The structures of the coatings were further examined using the X-ray diffractometer. Figure 5.3 shows the XRD data for the substrate temperatures of 150 and 350°C. The data for the other substrate temperatures are not shown as they all show very similar characteristics, that of (111) preferred orientation and only a small (or no) contribution from other planes.

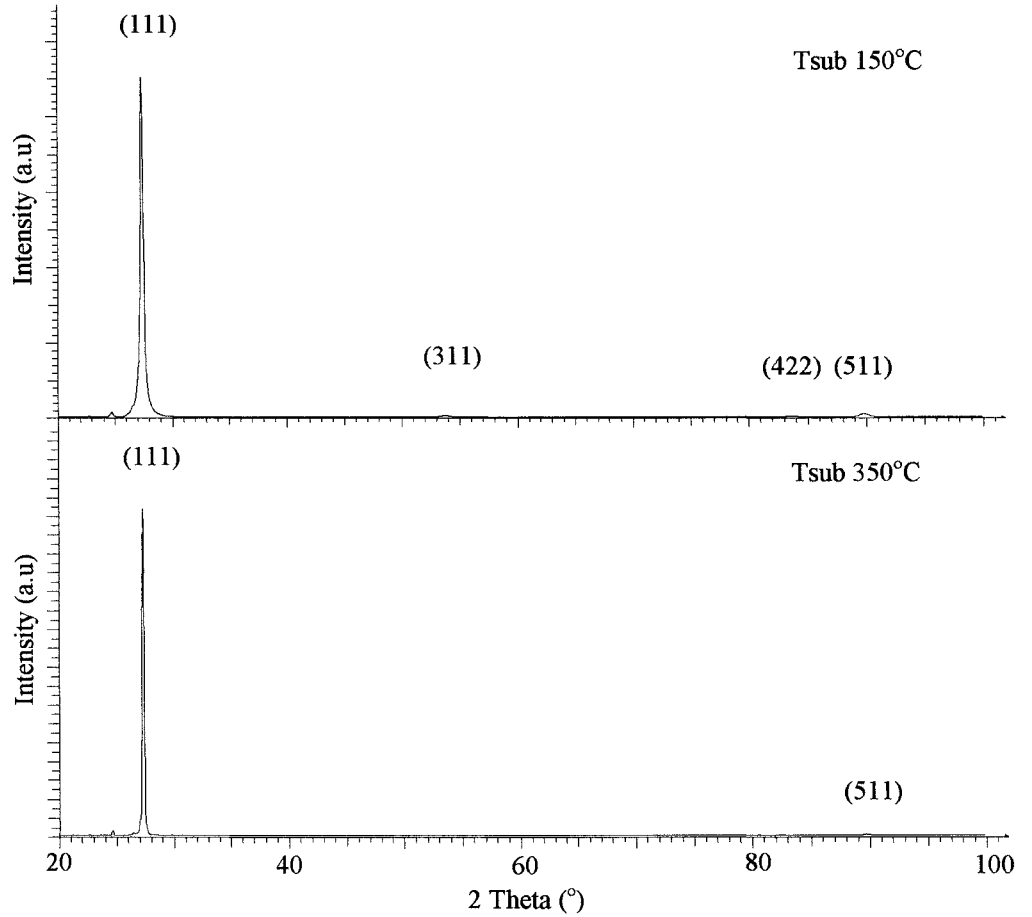


Figure 5.3. XRD Data of ZnSe Deposited with Parameters 25mm / T_{source} 600°C and Varying Substrate Temperature.

Crystallite size can also be estimated from the XRD data using the Scherrer technique (assuming negligible micro-strain) [5]. The line broadening of the planes is related to the crystallite size, L , perpendicular to the diffraction plane by

$$L = \frac{c\lambda}{B \cos \theta} \quad 5.1.$$

where c is a constant determined by the measurement method (0.94 in this case [5]), λ is the wavelength of the $\text{CuK}\alpha$ radiation ($1.5406 \times 10^{-10} \text{ m}$), B the broadening expressed

in radians due to the crystallite size (FWHM of peak) and θ the diffraction angle. The FWHM data used in these investigations were determined using the evaluation software (EVA) in the DiffracPlus 4.3 Basic software that is used to operate the X-ray diffractometer. Table 5.1 shows the crystallite size data determined using the Scherrer technique. Initially these data were plotted as a function of temperature to see if any trends could be displayed and a small increase in crystallite size with temperature was found. However, to produce a linear fit, errors bars in excess of 15% are required, which are much larger than can be reasonably estimated from the experimental errors ($\pm 3\%$ or $\sim 1\text{nm}$ from error in determining FWHM and accuracy in $\cos\theta$). In addition it should be noted that the Scherrer technique is more suitable for grading purposes and not necessarily for absolute measurements [6].

Substrate Temperature (°C)	Crystallite Size (nm)
100	31
150	28
200	37
250	41
300	41
350	44
400	37

Table 5.1. Crystallite Size Determined from XRD Data
for ZnSe Deposited with Parameters 25mm / $T_{\text{source}} 600^{\circ}\text{C}$.

Care must be taken when comparing the grain size estimations obtained from the SEM micrographs and that obtained using the XRD and Scherrer technique. The SEM grain (radius) sizes are extrapolated from measurements parallel to the plane of the film, whereas, the Scherrer technique uses XRD data perpendicular to the film plane. In addition, what each technique actually measures needs to be considered. The grains or particles observed by the SEM consist of one or more crystals and cannot be determined by XRD. On the other hand the Scherrer technique gives crystallite size which is equal or smaller to the crystal size. Therefore the SEM data indicate actual grain or particle growth with increasing substrate temperature. However, the Scherrer data shows the crystallite size remains reasonably constant.

5.2.2 Optical Properties of ZnSe - 25mm / T_{source} 600°C

The optical properties of the ZnSe coatings were investigated using an Hitachi U3000 Spectrophotometer, the operation of which is described in section 4.3.2.1. The transmittance data for a wavelength range of 400 to 800nm is shown in figure 5.4. The energy bandgap of ZnSe is 2.67eV [7], which in terms of wavelength is equivalent to ~460nm. The thickness of the coatings in figure 5.4 are all in the range 2 to 4 μm but the transmittance of some substrate temperatures (200 and 250°C) is much higher than others (100 and 400°C). This would suggest that the structure of the layers is affecting the optical properties of the coatings, however, this was not evident from the XRD data as all coatings showed a similar preferred (111) orientation.

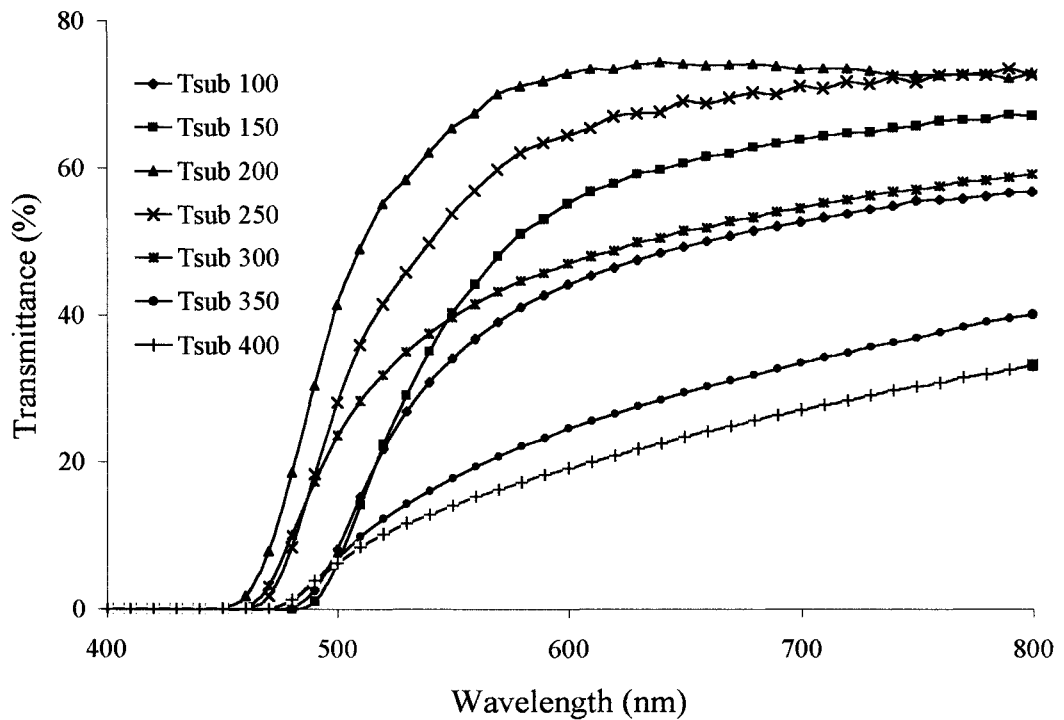


Figure 5.4. Transmittance as a Function of Wavelength for ZnSe Deposited with Parameters 25mm / T_{source} 600°C and Varying Substrate Temperature.

The energy bandgap can be calculated directly from the optical properties. For absorbent films with no interference fringes in the absorption edge, the transmittance and absorption coefficient are related by [8]

$$T = (1 - R)^2 \exp(-\alpha d) \quad 5.2.$$

where T and R are the transmittance and reflectance respectively, α is the absorption coefficient and d the thickness of the film. Equation 5.2 is only valid when the refractive index, n, of the coating is greater than the substrate. In all cases in this work, the refractive indices of the coating is larger than the substrate ($n_{\text{glass}} \sim 1.5$, $n_{\text{ZnSe}} \sim 2.5$, $n_{\text{ZnS}} \sim 2.4$ and $n_{\text{CdTe}} \sim 3.0$ depending upon wavelength) [9]. Also, if the assumption is made that the reflectance is low, equation 5.2 can be rewritten in terms of absorption coefficient as

$$\alpha \approx -\frac{1}{d} \ln T \quad 5.3.$$

The relationship between the energy bandgap and absorption coefficient is given by [10]

$$\alpha \approx \left(\frac{A}{h\nu} \right) (h\nu - E_g)^n \quad 5.4.$$

where A is a constant, $h\nu$ is the photon energy and n depends on the type of semiconductor bandgap. For direct bandgap semiconductors $n = 1/2$, whereas for indirect bandgap semiconductors $n = 3/2$. As all the materials in this work have a direct bandgap, plotting $(\alpha h\nu)^2$ versus $h\nu$ and extrapolating to the x axis gives the energy bandgap of the semiconductor under investigation. The energy bandgap of all layers were determined using this technique and a plot of two substrate temperatures (200 and 300°C) are shown in figure 5.5 (error in E_g estimated from method used to extrapolate data). It should be noted that the transmittance data in this case were recorded with data intervals of 1nm not 10nm as in figure 5.4.

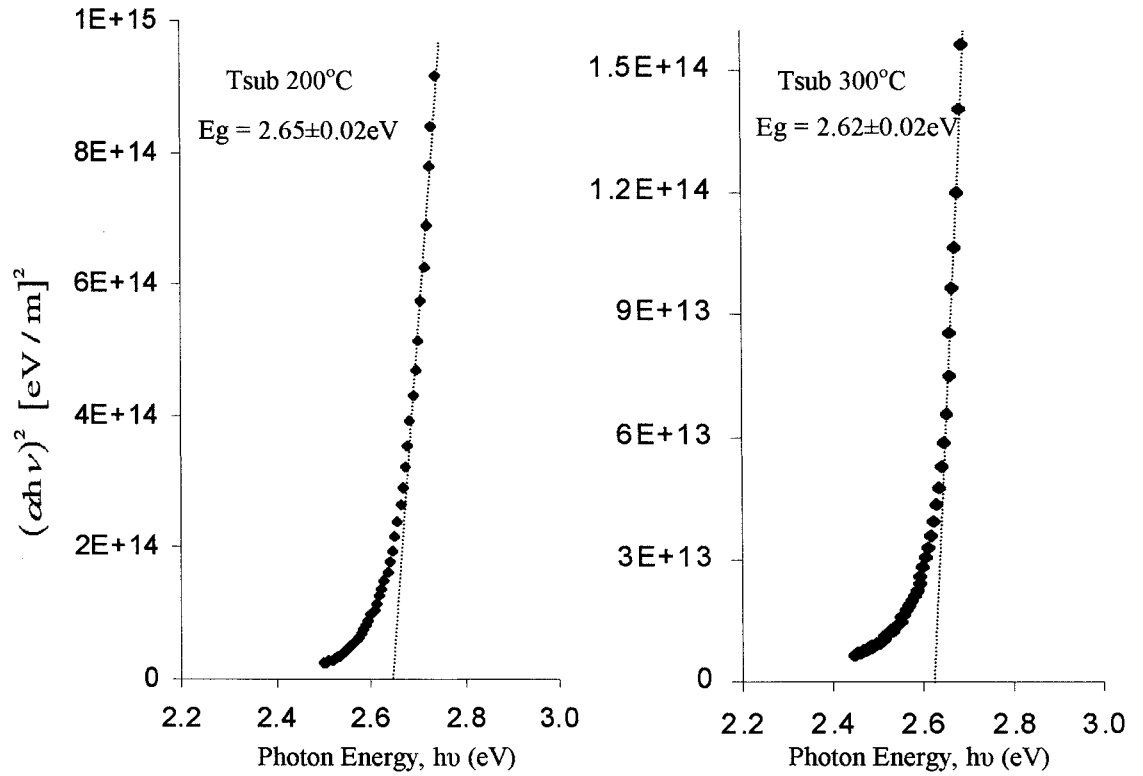


Figure 5.5. $(\alpha h\nu)^2$ as a Function of Photon Energy ($h\nu$) for ZnSe Deposited with Parameters 25mm / $T_{\text{source}} 600^\circ\text{C}$ and Varying Substrate Temperature.

A plot of energy bandgap versus substrate temperature is drawn in figure 5.6. These data would indicate that a preferred substrate temperature of 200 to 300°C (E_g 2.65 and 2.62eV) produces material with an energy bandgap close to 2.67eV. The difference in the lower energy gap values could be due to additional energy states that have been unintentionally introduced during layer growth. Such defects could act as recombination centres in devices and therefore adversely affect the photovoltaic performance of the cell.

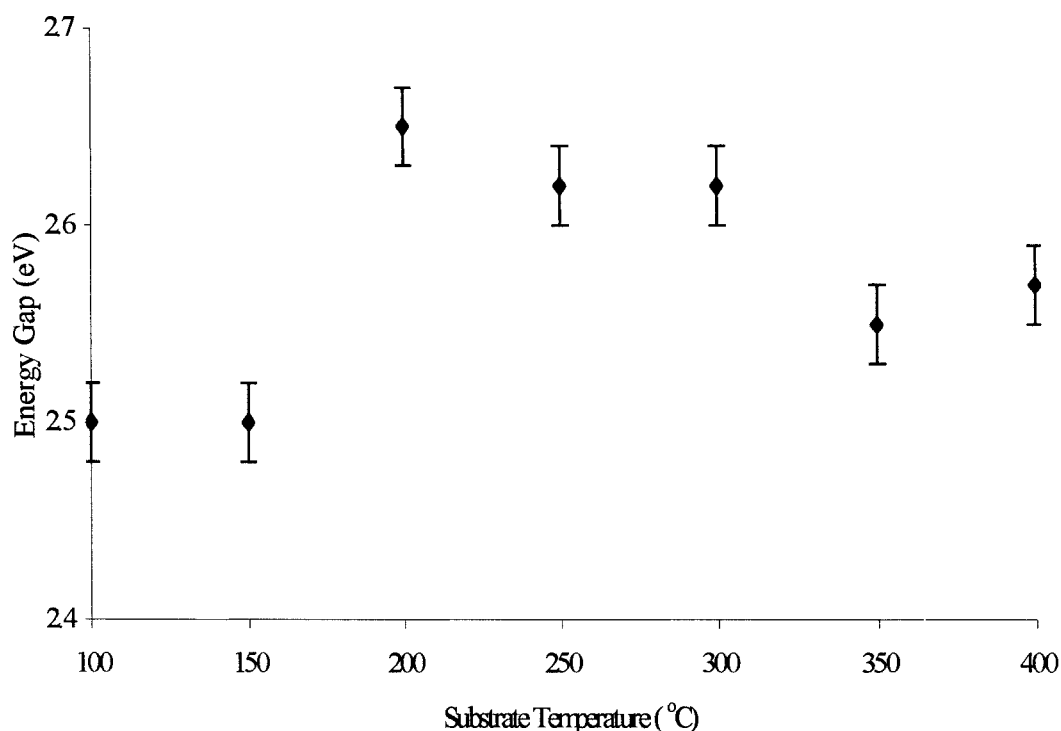


Figure 5.6. Energy Bandgap Versus Substrate Temperature Determined Using Optical Data for ZnSe Deposited with Parameters 25mm / T_{source} 600°C.

5.2.3 Structure of ZnSe - 11mm / T_{source} 600°C

Using the same sample preparation, material preparation and deposition techniques, a further investigation was conducted with a source - substrate distance of 11mm. Due to the mechanical configuration of the plant, 11mm was the closest distance that could be achieved, while still allowing twin source evaporation (of buffer and absorber layer) in the same chamber without breaking vacuum and in addition to allowing independent shutter control.

In reducing the source substrate distance, the morphology of the coatings has altered, figure 5.7a and 5.7b. An increase in grain size with increasing substrate temperature is found, which is confirmed by the plot of average grain radius versus substrate temperature in figure 5.8. In addition, there is an increase in grain size when compared with the morphology of the SEM micrographs with a source – substrate distance of 25mm (section 5.2.1).

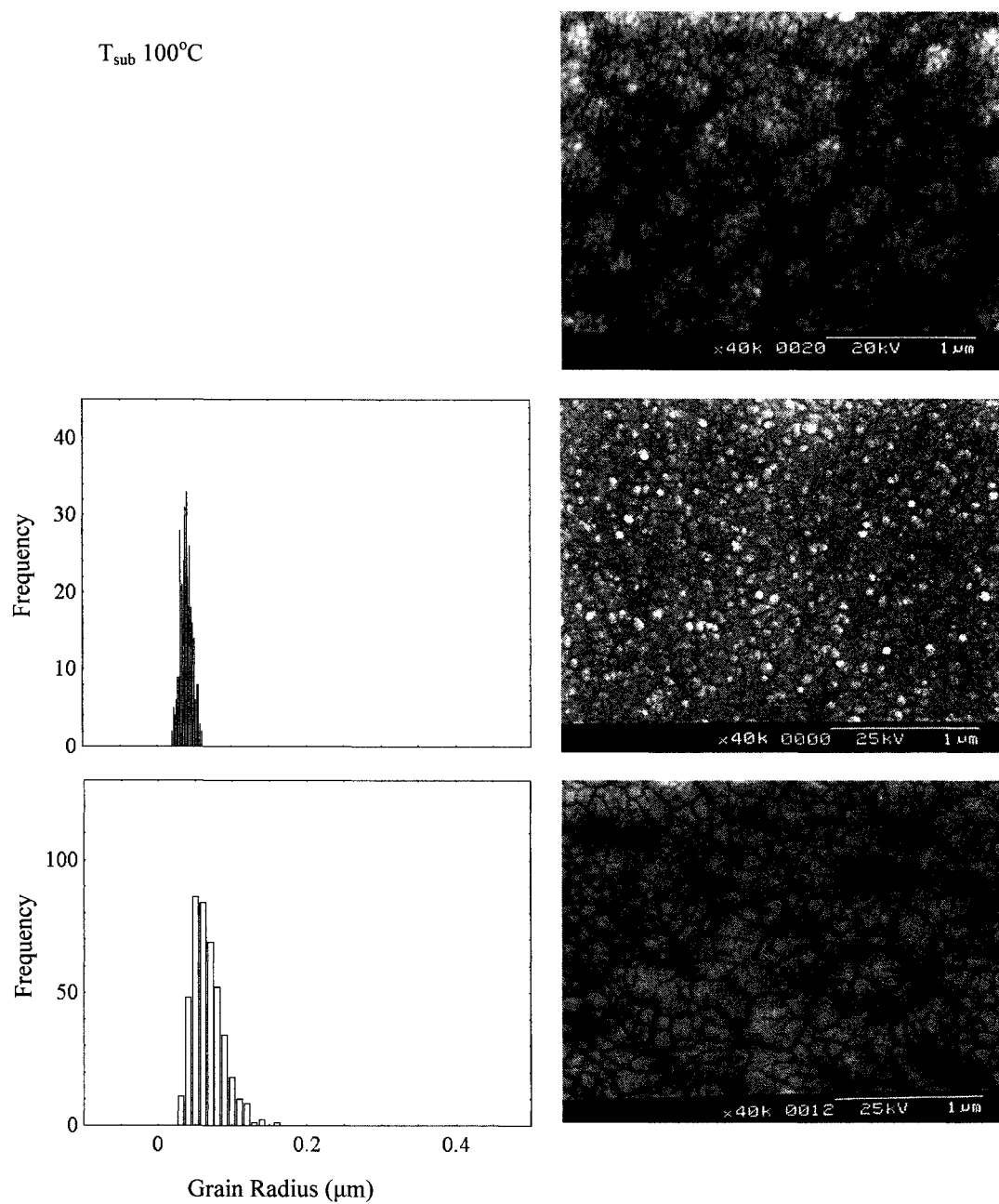


Figure 5.7a. SEM Micrographs of ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^{\circ}\text{C}$ and Varying Substrate Temperature.

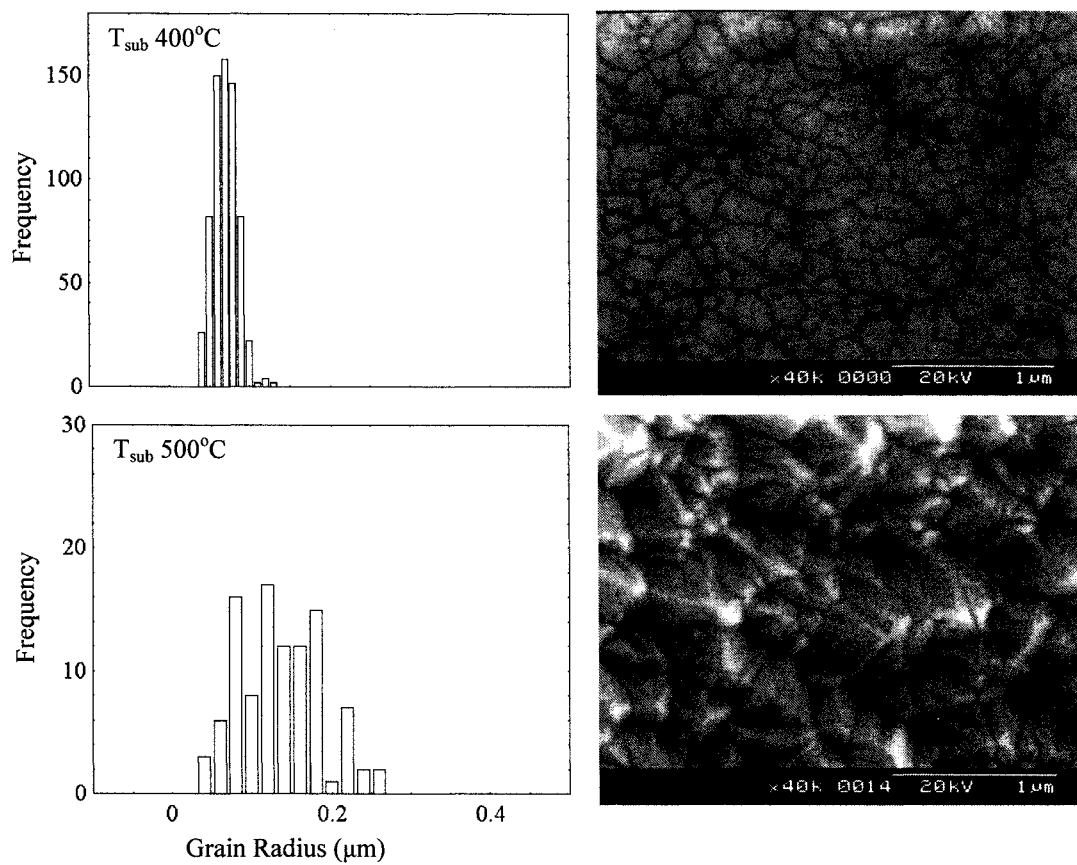


Figure 5.7b. SEM Micrographs of ZnSe Deposited with Parameters 11mm / $T_{\text{source}} = 600^{\circ}\text{C}$ and Varying Substrate Temperature.

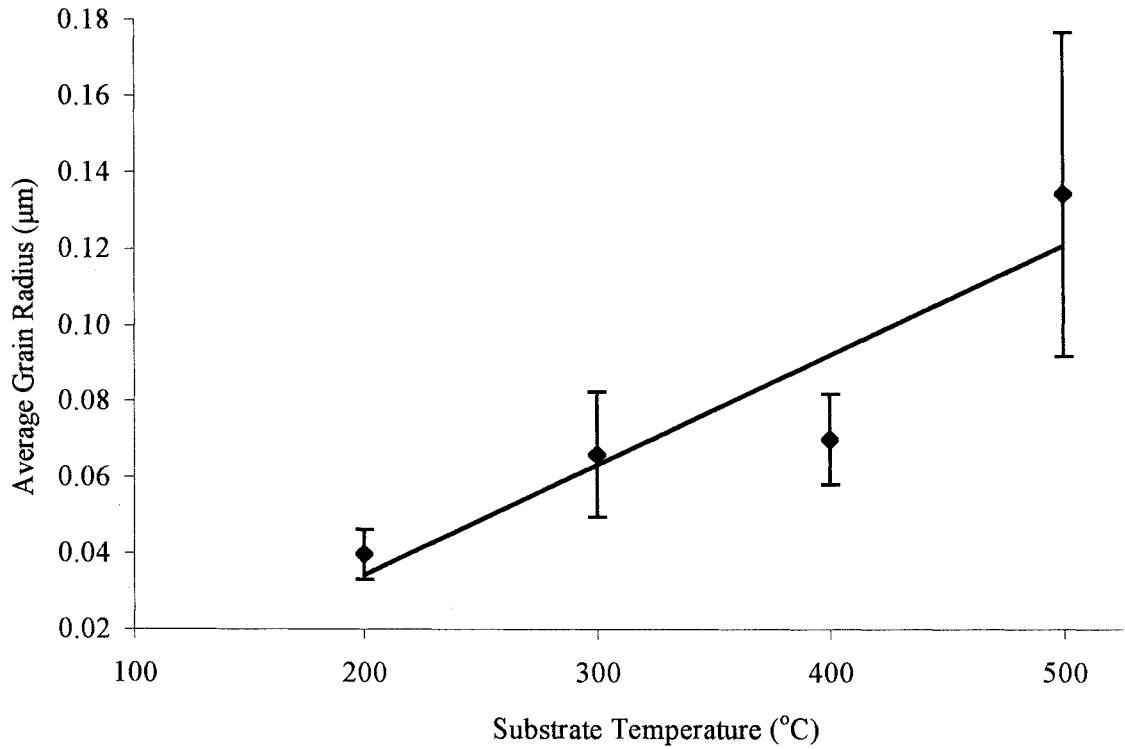


Figure 5.8. Average Grain Radius Versus Substrate Temperature for ZnSe Deposited with Parameters 11mm / T_{source} 600°C.

The XRD data for two of the deposited layers are shown in figure 5.9. The data for the substrate temperature of 100°C indicates a contribution from other planes but for all the other substrate temperatures, a preferred orientation along the (111) plane is found (all virtually identical to the T_{sub} 300°C data and therefore not shown). The crystallite size determined from the XRD data, of table 5.2, shows a gradual increase in size with increasing substrate temperature. As with the data in table 5.1, it is difficult to justify the large errors that would be needed to fit the data (> 10 to 15%) and therefore the main source of error is considered to be the technique itself.

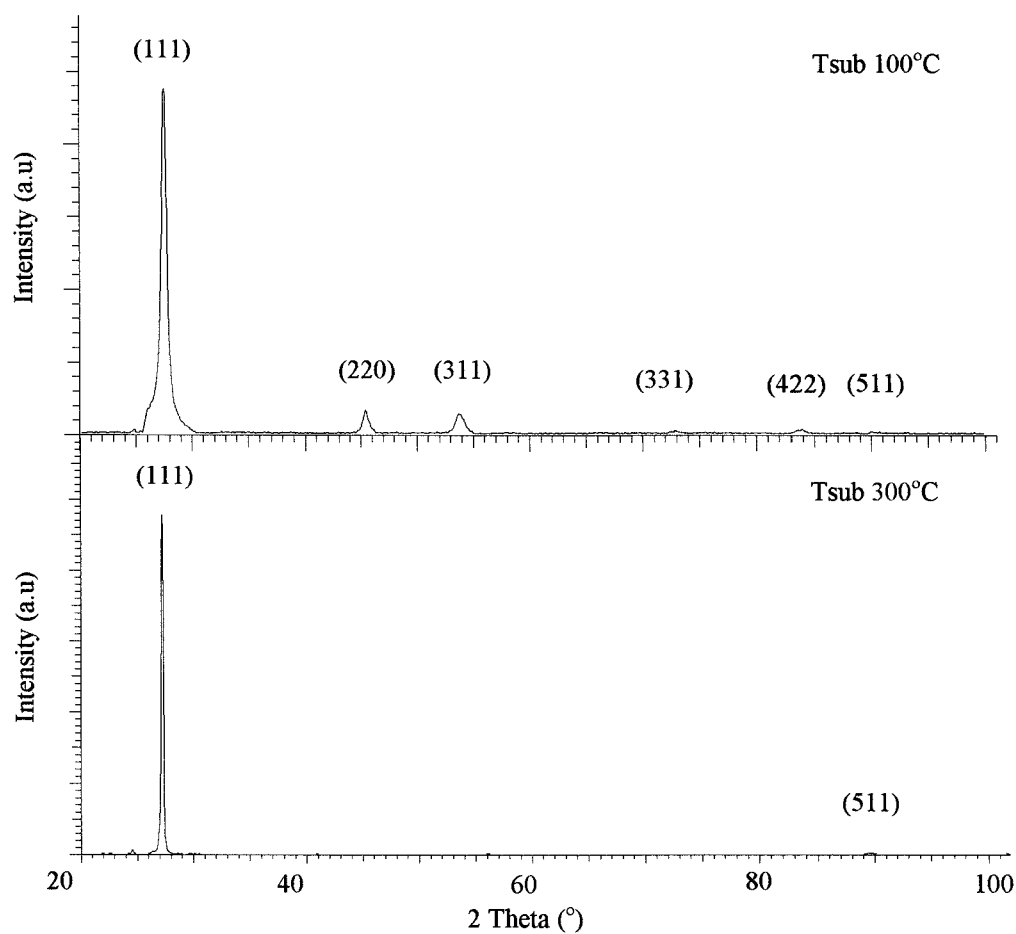


Figure 5.9. XRD Data of ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ and Varying Substrate Temperature.

Substrate Temperature ($^\circ\text{C}$)	Crystallite Size (nm)
100	16
200	29
300	41
400	35
500	43

Table 5.2. Crystallite Size Determined from XRD Data for ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$.

5.2.4 Optical Properties of ZnSe – 11mm / $T_{\text{source}} 600^{\circ}\text{C}$

The transmittance data for the source – substrate distance of 11mm are shown in figure 5.10. These layers are approximately 2 to 4 μm thick but unlike the 25mm data, (section 5.2.2) the transmittance is similar across the whole range above the absorption edge. The energy bandgap was again determined using equation 5.4 and the data for the 200 and 300 $^{\circ}\text{C}$ samples are plotted in figure 5.11. The plot of figure 5.12 illustrates the energy bandgap as a function of substrate temperature. These data show an increase across the range of energy bandgap when compared to the 25mm data. Also, the substrate temperatures indicating the best properties in terms of transmittance and bandgap are found to be in the range 200 to 300 $^{\circ}\text{C}$.

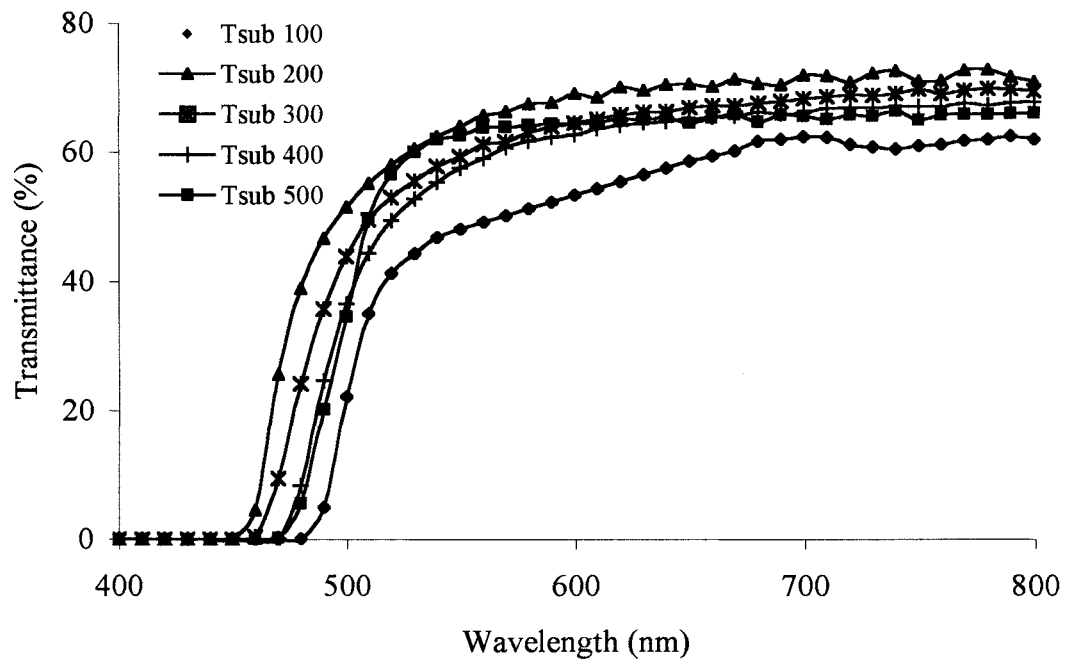


Figure 5.10. Transmittance as a Function of Wavelength for ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^{\circ}\text{C}$ and Varying Substrate Temperature.

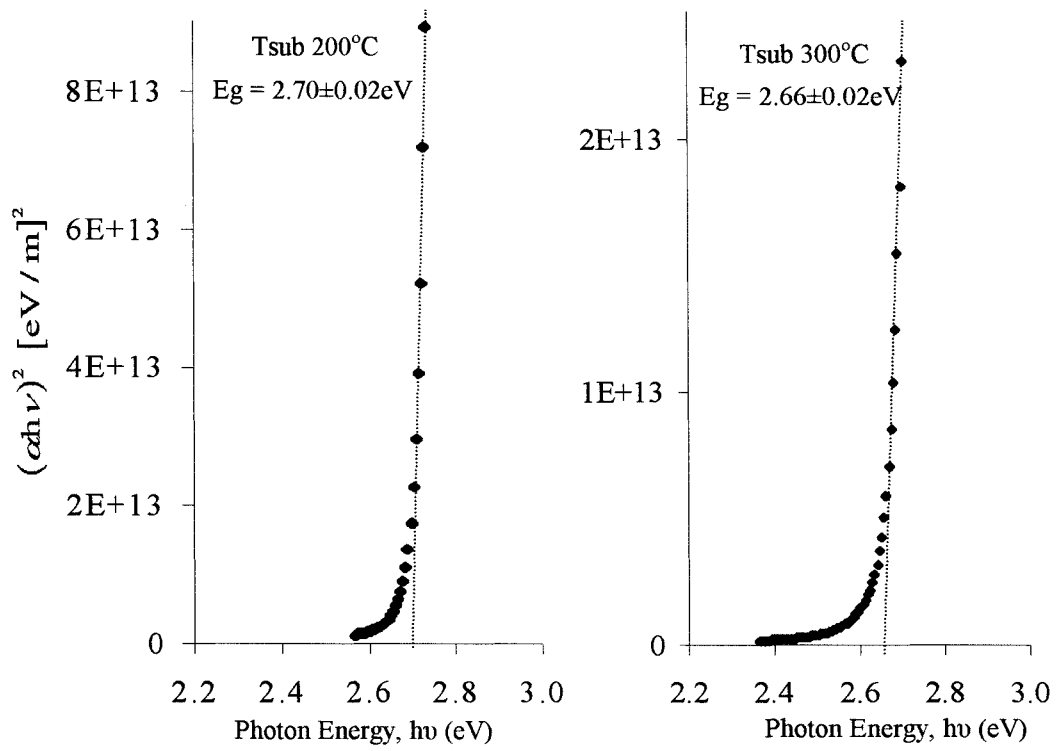


Figure 5.11. $(\alpha h\nu)^2$ as a Function of Photon Energy ($h\nu$) for ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ and Varying Substrate Temperature.

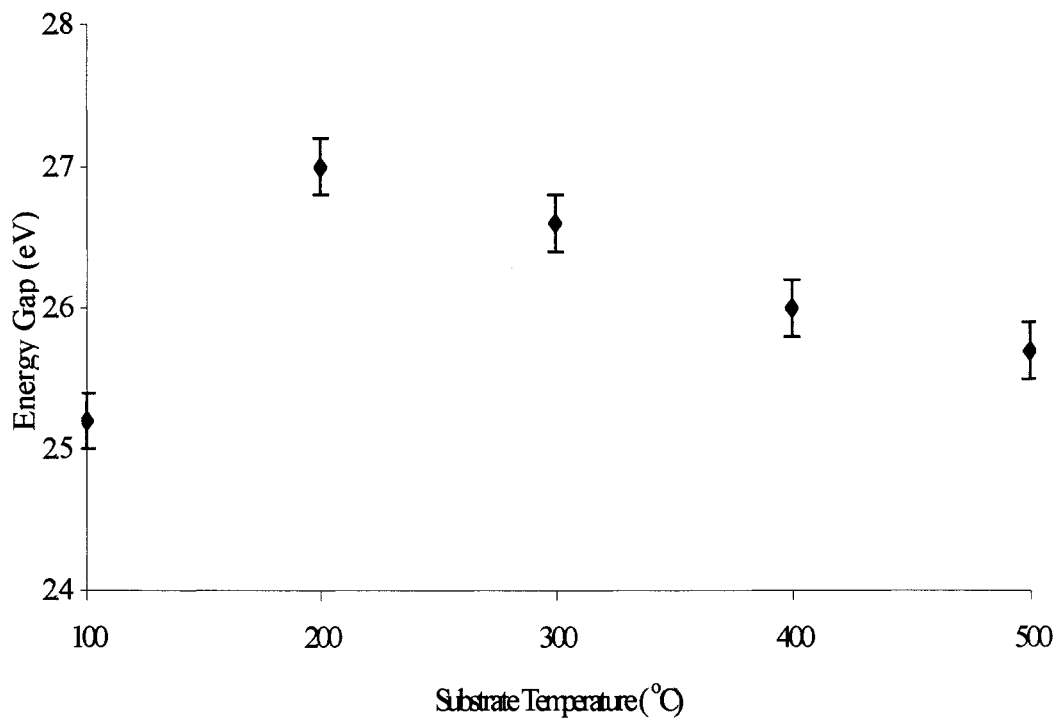


Figure 5.12. Energy Bandgap Versus Substrate Temperature Determined Using Optical Data for ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$.

5.2.5 Structure of ZnSe - 11mm / T_{source} 600°C / Baffle

In the previous sections, an investigation was undertaken to determine the parameters that will produce the best layers in terms of structure and optical properties, that would enable application in solar cells fabricated using this system. A problem with some of the coatings, previously discussed in sections 5.2.1 to 5.2.4, was the surface integrity. The evaporation powder was placed in a quartz crucible into which quartz wool was added, however, in some cases pinholes were still found. It was therefore decided to use a further mechanical obstacle to the vapour path by introducing a baffle. The baffle was manufactured using tantalum and was placed on top of the heater, allowing the source – substrate distance to remain as 11mm.

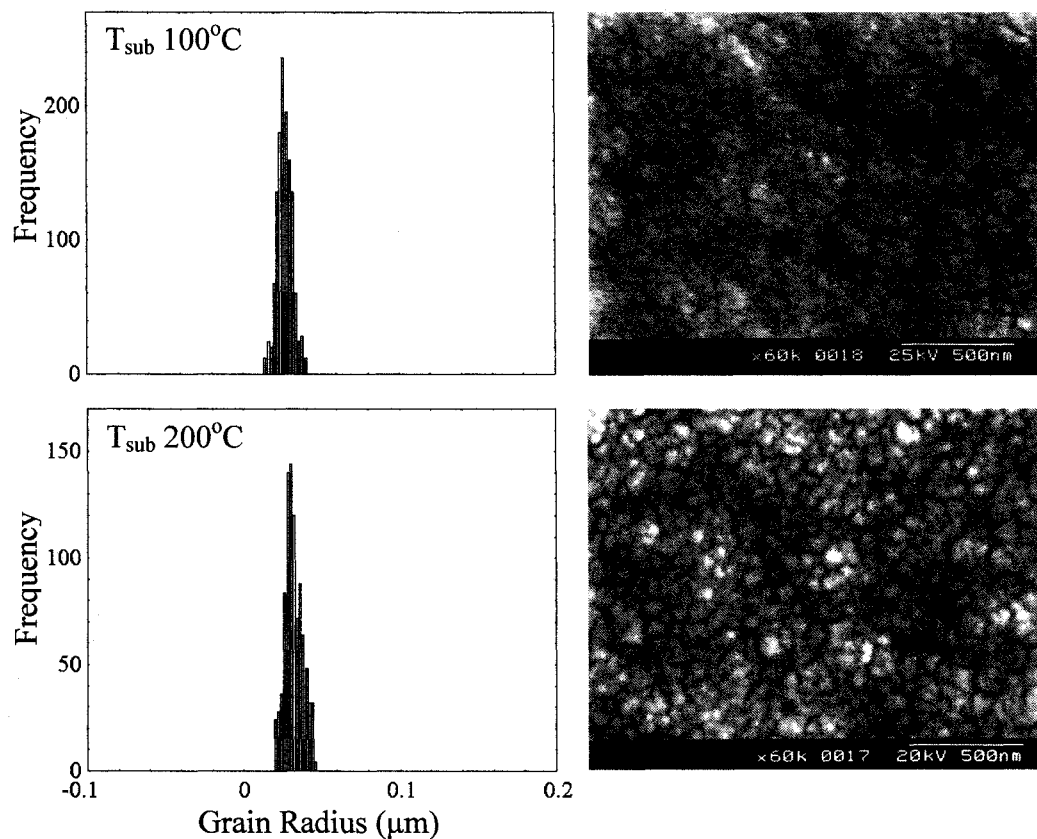


Figure 5.13a. SEM Micrographs of ZnSe Deposited with Parameters 11mm / T_{source} 600°C / Baffle and Varying Substrate Temperature.

The SEM micrographs and corresponding histograms for a distance of 11mm, and the addition of a baffle, are shown in figures 5.13a and 5.13b. Once again there is an increase in grain size with increasing substrate temperature. The average grain radii, of figure 5.14, confirm the interpretation from the micrographs but also demonstrate a decrease in radius when compared to the data without the baffle (figure 5.8). Therefore, the increase in path length for the gaseous materials must affect the morphology of the layers.

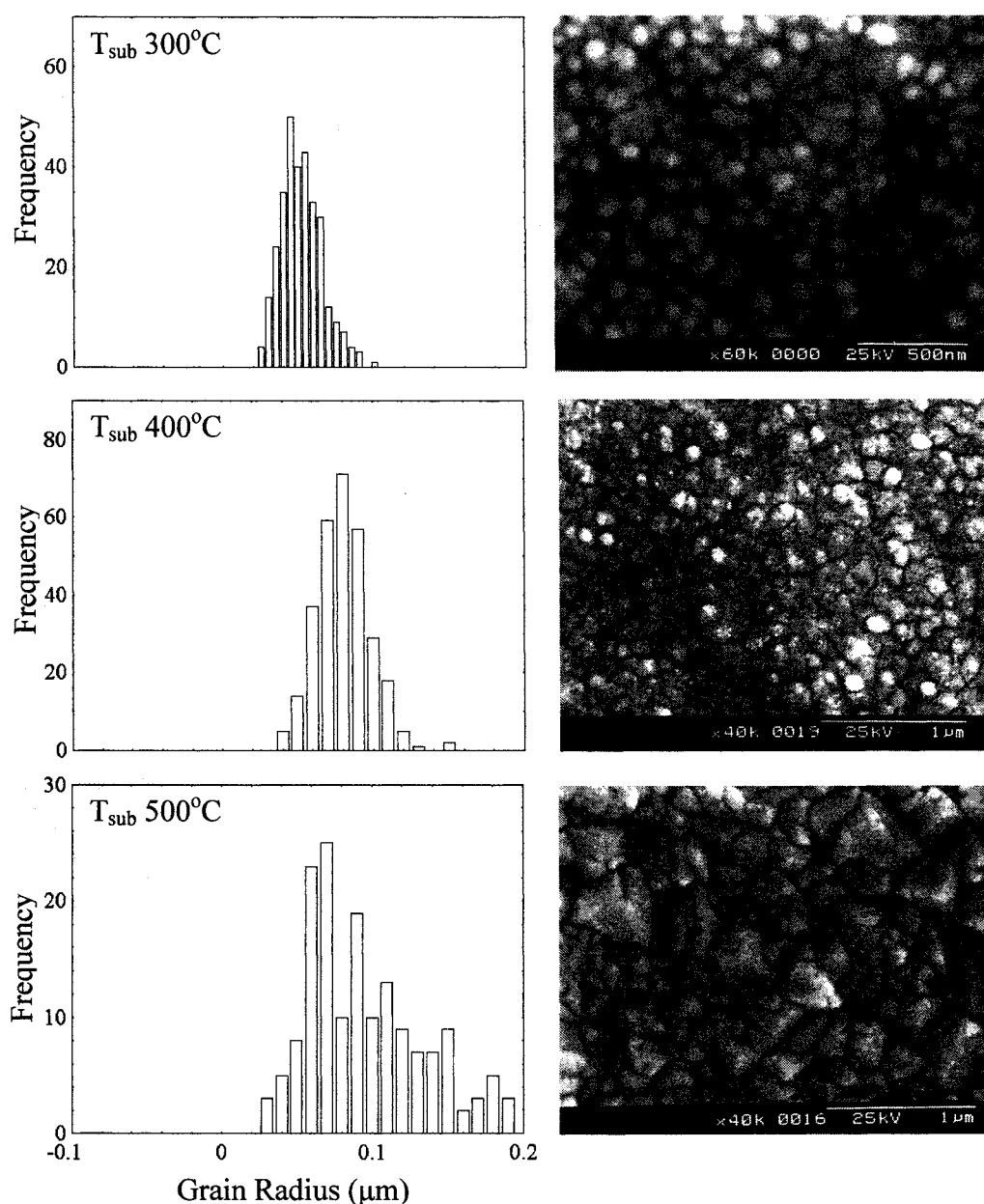


Figure 5.13b. SEM Micrographs of ZnSe Deposited with Parameters 11mm / T_{source} 600°C / Baffle and Varying Substrate Temperature.

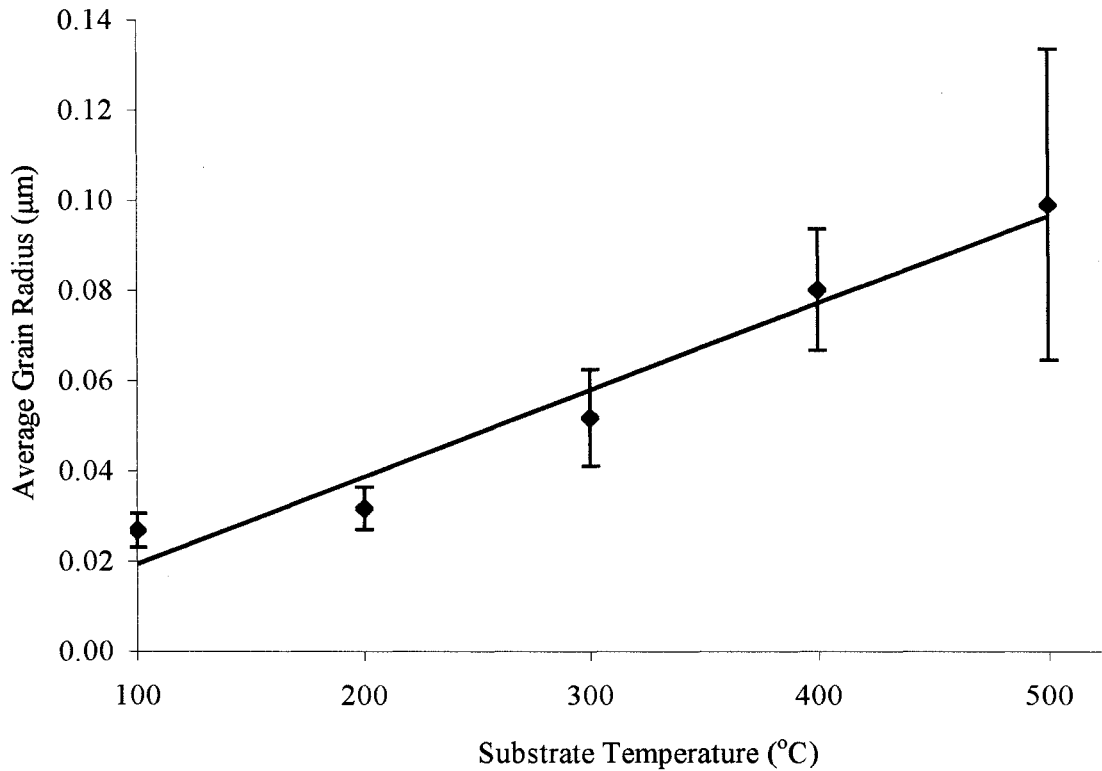


Figure 5.14. Average Grain Radius Versus Substrate Temperature for ZnSe Deposited with Parameters 11mm / T_{source} 600°C / Baffle.

The XRD data, figure 5.15, again indicates a preferred orientation on the (111) plane and again little contribution from other planes (not all XRD data shown but other data are identical to T_{sub} 500°C). The crystallite size obtained from the diffraction data was calculated using equation 5.1 and is tabulated in 5.3. In comparison, unlike the SEM data of figure 5.14, the crystallite size determined from the XRD data is almost constant with increasing substrate temperature. This agrees with the data of sections 5.2.1. and 5.2.3. where the SEM observations show an increase in grain size with increasing substrate temperature, whereas the XRD determination indicate a constant / slight increase in crystallite size with increasing substrate temperature.

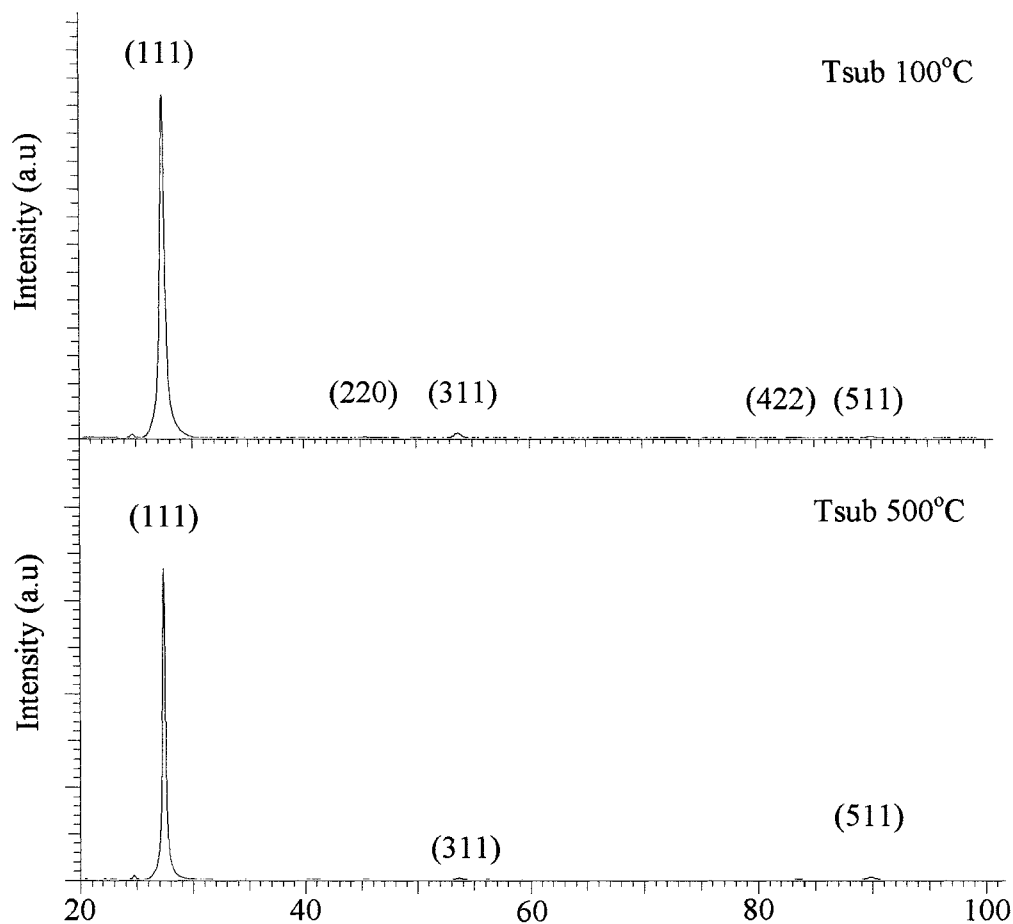


Figure 5.15. XRD Data of ZnSe Deposited with Parameters 11mm / T_{source} 600°C / Baffle and Varying Substrate Temperature.

Substrate Temperature (°C)	Crystallite Size (nm)
100	20
200	26
300	21
400	24
500	22

Table 5.3. Crystallite Size Determined from XRD Data for ZnSe Deposited with Parameters 11mm / T_{source} 600°C / Baffle.

5.2.6 Optical Properties of ZnSe – 11mm / T_{source} 600°C / Baffle

The transmittance data for the coatings, including a baffle, are plotted in figure 5.16. The data for T_{sub} 200°C again appears to show the best optical properties in that the absorption edge is close to the accepted value of 460nm (or 2.67eV). The energy bandgap obtained from the plots of $(\alpha h\nu)^2$ versus $h\nu$ (figure 5.17) are shown as a function of substrate temperature in figure 5.18. This confirms the assumption from the transmittance data that a substrate temperature of 200°C is preferred for producing an energy bandgap close to the accepted value, and in addition, has the highest transmittance above the absorption edge.

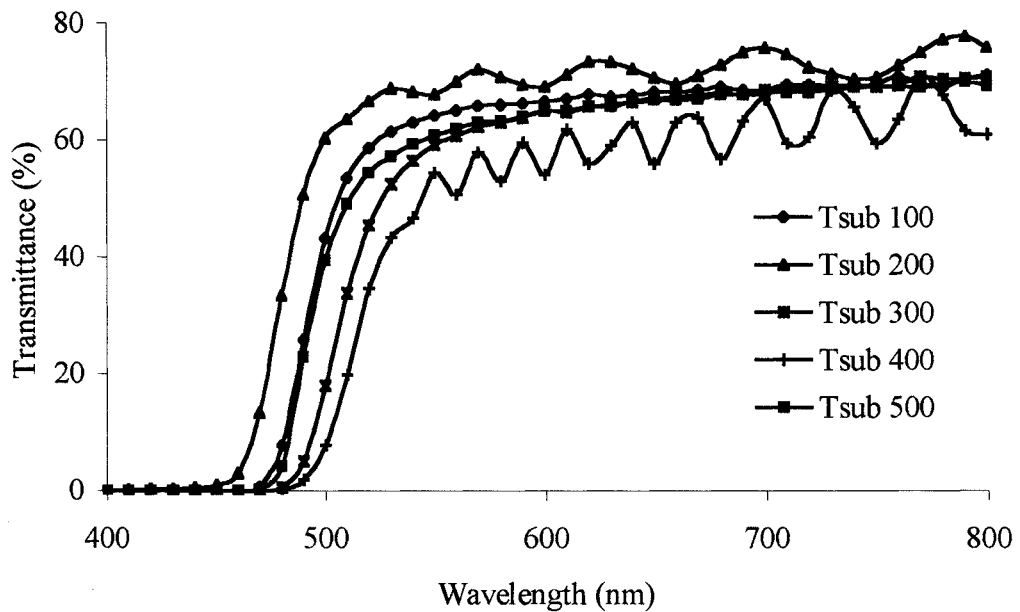


Figure 5.16. Transmittance as a Function of Wavelength for ZnSe Deposited with Parameters 11mm / T_{source} 600°C / Baffle and Varying Substrate Temperature.

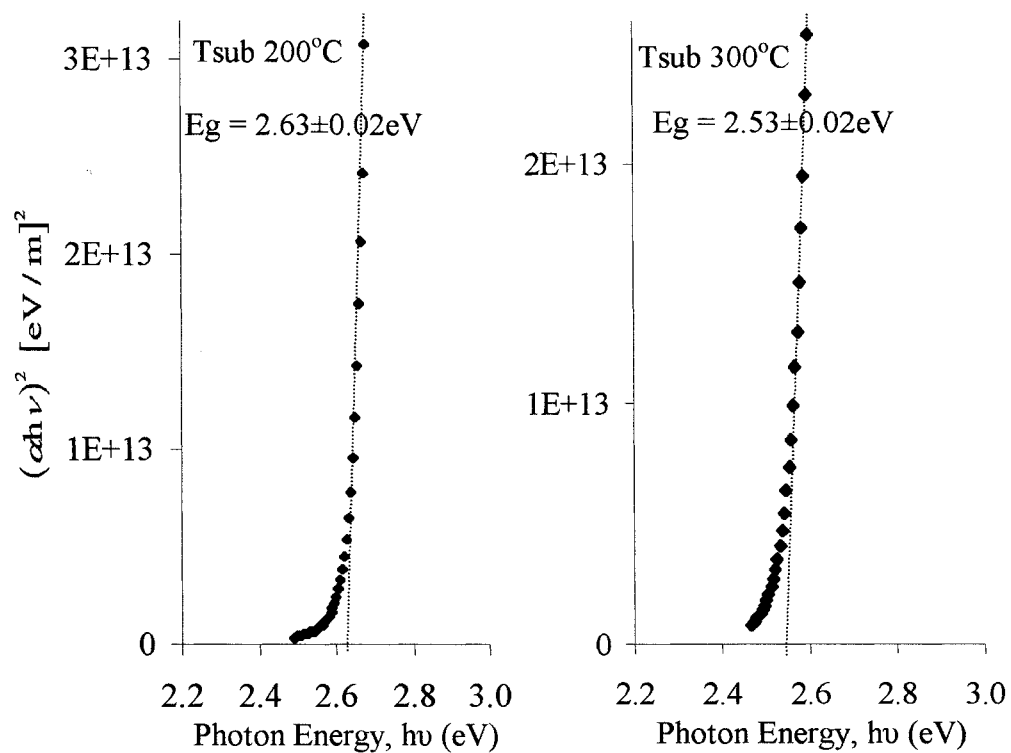


Figure 5.17. $(\alpha h\nu)^2$ as a Function of Photon Energy ($h\nu$) for ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / Baffle and Varying Substrate Temperature.

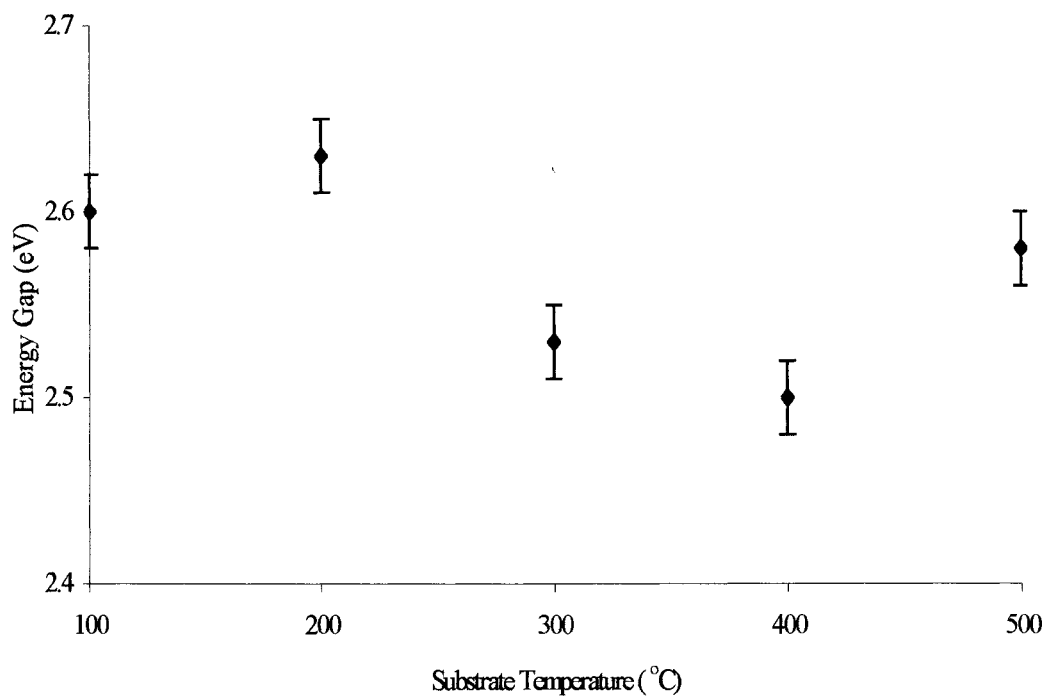


Figure 5.18. Energy Bandgap Versus Substrate Temperature Determined Using Optical Data for ZnSe Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / Baffle.

5.2.7 Structure of $\text{ZnS}_x\text{Se}_{1-x}$ - 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle

An important aspect with ternary alloys such as $\text{ZnS}_x\text{Se}_{1-x}$ is the relationship between the end binary alloys (i.e. ZnS and ZnSe) and their mixed crystal properties. This is important not only in terms of lattice matching but also in bandgap engineering of heterojunction devices. In some cases a linear relationship between the end binaries can be found, whereas with other properties there is a non-linear relationship (see section 3.2). Another consideration is the effect the deposition / growth technique has on the structural, electrical and optical properties of the mixed ternary system.

The ZnSe data from sections 5.2.1 to 5.2.6 was reviewed in order to find suitable deposition conditions to produce $\text{ZnS}_x\text{Se}_{1-x}$ layers. It was concluded that the tantalum baffle was required to reduce the risk of pinholes. The higher substrate temperatures produced larger grains, which are believed to be beneficial to photovoltaic conversion by reducing grain boundary effects (more so in absorber than buffer layers) [11]. However, these layers indicated signs of potential recombination sites, due to reduced longer wavelength absorption edges and lower energy bandgaps. Therefore it was concluded that the lower substrate temperature of 200°C had the potential to produce better quality layers for PV applications. In addition, when the buffer layers are fabricated with the absorber layers (CdTe), a post deposition heat treatment is required which has been shown to induce grain growth in not only the CdTe, but also the CdS buffers layers [12, 13]. However, if thin buffer layers are required, as in many thin film solar cells, then small grain sizes are desired in order to obtain continuous pinhole free layers [14]

The $\text{ZnS}_x\text{Se}_{1-x}$ powders for evaporation were mixed by mass from the two end binary, namely ZnSe and ZnS (purity 99.999% purchased from Johnson Matthey). The evaporant was again placed in a bottle shaped crucible with the addition of quartz wool. The evaporation procedure was identical to that of the previous sections, including a gentle outgas of the source (for ZnS) as recommended by [15].

To determine the alloy composition of the $\text{ZnS}_x\text{Se}_{1-x}$ layers, two processes were investigated. The first method employed to determine the alloy composition used the X-ray diffraction data. If this alloy system obeys Vegards law, then according to equation 3.22, there should be a linear relationship between the lattice

constants of the two end binary compounds. Therefore by measuring the d spacings from the diffraction pattern, the lattice constant for each plane can be calculated using equation 4.3 (for cubic systems) and the x value extrapolated. The original weight fractions of the source components, the measured d spacings, calculated lattice constants and extrapolated alloy compositions are summarised in table 5.4 (error in alloy composition from standard deviation of extrapolation uncertainty). The actual d-spacing values of table 5.4 were determined using the EVA software on an extended 2 theta scale. The difference in original weight fraction and final composition could be due to the different vapour pressure temperatures of the two compounds. For ZnSe this is 660°C at 10⁻⁴ Torr, whereas for ZnS it is ~800°C (sublimes) at 10⁻⁴ Torr [15]. The diffraction data for the six alloy compositions of table 5.4 are shown in figures 5.19a and 5.19b.

ZnSe powder (wt %)	ZnS powder (wt %)	(111) peak d (Å)	(111) peak a (Å)	(311) peak d (Å)	(311) peak a (Å)	x value (±0.02)
100	0	3.28	5.68	1.71	5.67	0
75	25	3.23	5.59	1.69	5.61	0.27
50	50	3.21	5.56	1.67	5.54	0.45
25	75	3.18	5.51	1.66	5.51	0.60
10	90	3.14	5.44	1.64	5.44	0.86
0	100	3.12	5.40	-	-	1.00

Table 5.4 Original Powder Weight Fractions, d Spacings, Lattice Constants and Alloy Composition, x, for ZnS_xSe_{1-x} Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

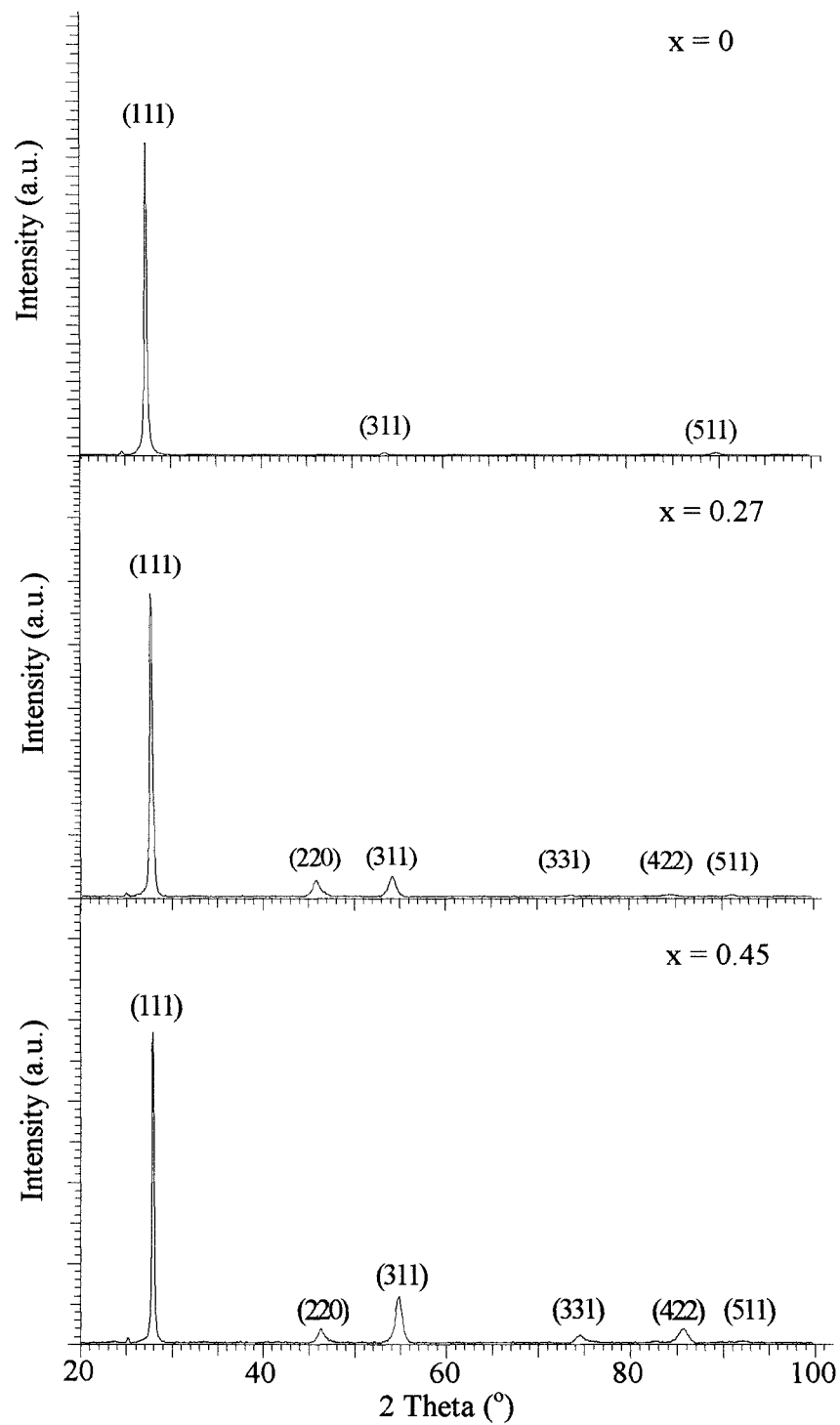


Figure 5.19a. XRD Data of $\text{ZnS}_x\text{Se}_{1-x}$ Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

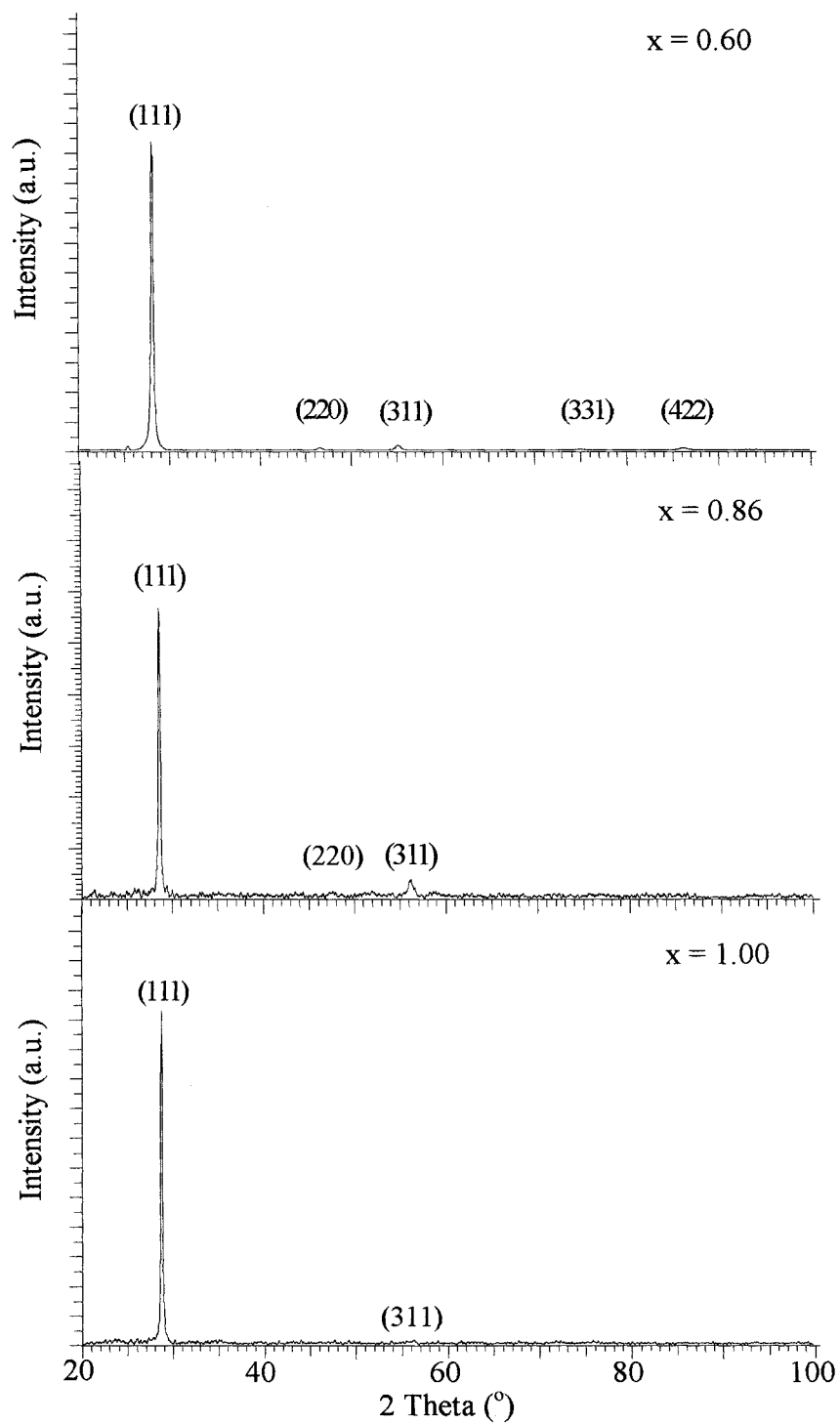


Figure 5.19b. XRD Data of ZnS_xSe_{1-x} Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

To illustrate the systematic shift in alloy composition, assuming linear lattice parameters, the normalised (111) peaks of the $\text{ZnS}_x\text{Se}_{1-x}$ alloys were plotted on an expanded 2 theta scale, figure 5.20.

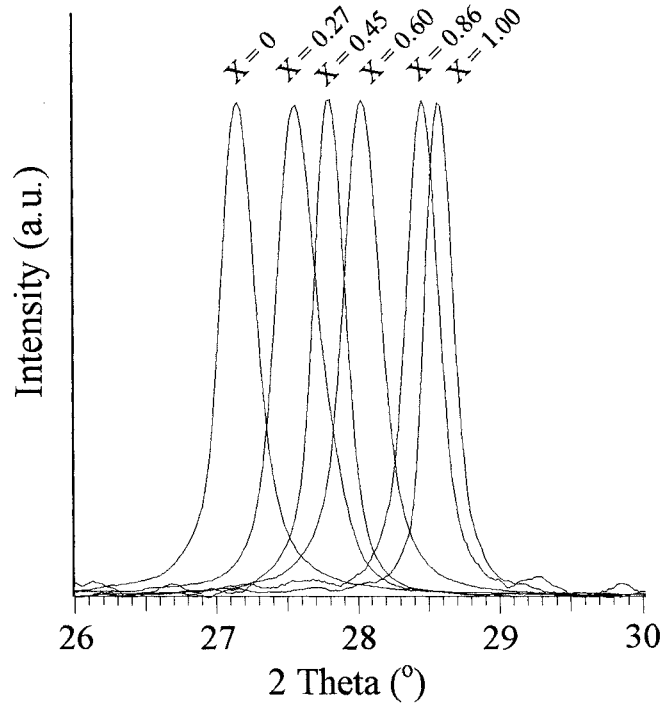


Figure 5.20. XRD Data of the Normalised (111) Peak of $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

A second method used to investigate the alloy composition used EDS analysis obtained using the electron microscope, table 5.5 (it should be noted that calibration of the EDS system was achieved using elemental Zn, S and Se). The stoichiometry of the ZnSe compares favourably with single crystal (Zn 56 at.% / Se 44 at.%) and CSS grown (Zn 55 ± 0.5 at.% / Se 44 ± 0.5 at.%) reported by [16]. Other workers have successfully determined the alloy composition of $\text{ZnS}_x\text{Se}_{1-x}$, grown with more sophisticated deposition methods, using EDS (MOCVD [17], sputtering [18]). These data show a stoichiometry of cation 50 at.% and anion 50 at.%. However, the data of table 5.5 did not produce results that agreed with the perceived alloy composition

intuitively taken from the optical data, calculated energy bandgaps (see section 5.2.8) and the deposition colour (it was found that the ZnSe coatings were coloured orange, the ZnS a milky white and the mixed powders a variation between the two). It is postulated that since the alloys were fabricated using binary compounds, the new system must be a function of the end binaries and not the combination of three individual alloys (discussed in section 3.2). It should also be noted that a direct relationship between the source compounds and EDS data may not be found as the stoichiometry is related to the molar fraction and not the weight fraction (of the source compounds).

ZnSe powder (wt %)	ZnS powder (wt %)	Zn (Atom %)	S (Atom %)	Se (Atom %)	x from XRD (± 0.02)
100	0	54	0	46	0
75	25	42	38	20	0.27
50	50	47	34	19	0.45
25	75	42	46	12	0.60
10	90	41	55	4	0.86
0	100	43	57	0	1.00

Table 5.5 EDS Analysis of Zn, S and Se for $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

The grain size from the diffraction data was again calculated using equation 5.1 across the alloy system, table 5.6. As with the data of tables 5.1 to 5.3, the uncertainty in the measurement is too small to allow a fit of this plotted data. However, this data does indicate a small increase in crystallite size with larger values of x in this alloy system.

Alloy Composition, x (± 0.02)	Crystallite Size (nm)
0	26
0.27	26
0.45	35
0.60	30
0.86	35
1.00	40

Table 5.6. Crystallite Size Determined from XRD Data of $\text{ZnS}_x\text{Se}_{1-x}$.
Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

To further investigate the diffraction data, the texture coefficient can be calculated. The Harris method, which was originally applied to rolled uranium, allows the degree of preferred orientation to be determined [19]

$$TC_i = \frac{I/I_o}{(1/N)\sum_N I/I_o} \quad 5.5.$$

where I is the measured peak intensity, I_o is the peak intensity of a random powder (obtained from the powder diffraction data – pdf release 1998, data sets 1 - 48 plus 70 - 85) and N is the number of reflections. For a random grain orientation, TC_i is equal to 1 and where $TC_i > 1$, there is a preferred orientation. The degree of orientation can be obtained by calculating the standard deviation using [20]

$$\sigma = \left(\frac{\sum_N (TC_i - TC_r)^2}{N} \right)^{1/2} \quad 5.6.$$

where TC_r is the random sample and therefore can be replaced by 1. If the standard deviation is not equal to zero, there is a preferred orientation. The calculated texture coefficients and standard deviations are presented in table 5.7. As a linear relationship between the end binaries is assumed, this was also extended to the powder diffraction file (pdf) data for the ZnSe and ZnS. These data indicate a preferred (111) orientation

across all alloys. For mixed binaries, the addition of peaks has reduced the texture coefficient of the (111) and reduced the standard deviation.

(hkl)	111	220	311	331	422	511	N = 6
<i>ZnSe Pdf (%)</i>	<i>1.00</i>	<i>0.65</i>	<i>0.37</i>	<i>0.12</i>	<i>0.13</i>	<i>0.07</i>	
<i>ZnS Pdf (%)</i>	<i>1.00</i>	<i>0.51</i>	<i>0.30</i>	<i>0.09</i>	<i>0.09</i>	<i>0.05</i>	
x							σ
0	5.031	-	0.154	-	-	0.815	1.683
0.27	3.338	0.342	0.696	0.416	0.488	0.720	1.055
0.45	2.440	0.207	1.105	0.702	1.085	0.460	0.719
0.60	4.460	0.118	0.304	0.490	0.628	-	1.508
0.86	4.771	0.233	0.996	-	-	-	1.571
1.00	5.676	-	0.324	-	-	-	1.929

Table 5.7. Texture Coefficient Determined from XRD Data for $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

The scanning electron microscope was again used to study the structure of the as deposited $\text{ZnS}_x\text{Se}_{1-x}$ coatings. The micrographs and histograms of figure 5.21a and 5.21b show how the grain sizes of the coatings generally increase with alloy composition, x. The average grain radius was calculated using the same technique as discussed in section 5.2.1., the results of which are plotted in figure 5.22. This indicates a general trend of increased grain size, with increasing x in the alloy $\text{ZnS}_x\text{Se}_{1-x}$.

The structure of the coatings was also investigated using an atomic force microscope (AFM), with the micrographs shown in figure 5.23. The grains of the observed layers show a systematic increase in size with increasing x value confirming the data from the SEM. These layers are compact and free from pinholes, which was corroborated using lower magnification on the SEM, the structure of which is essential to good solar cell device performance.

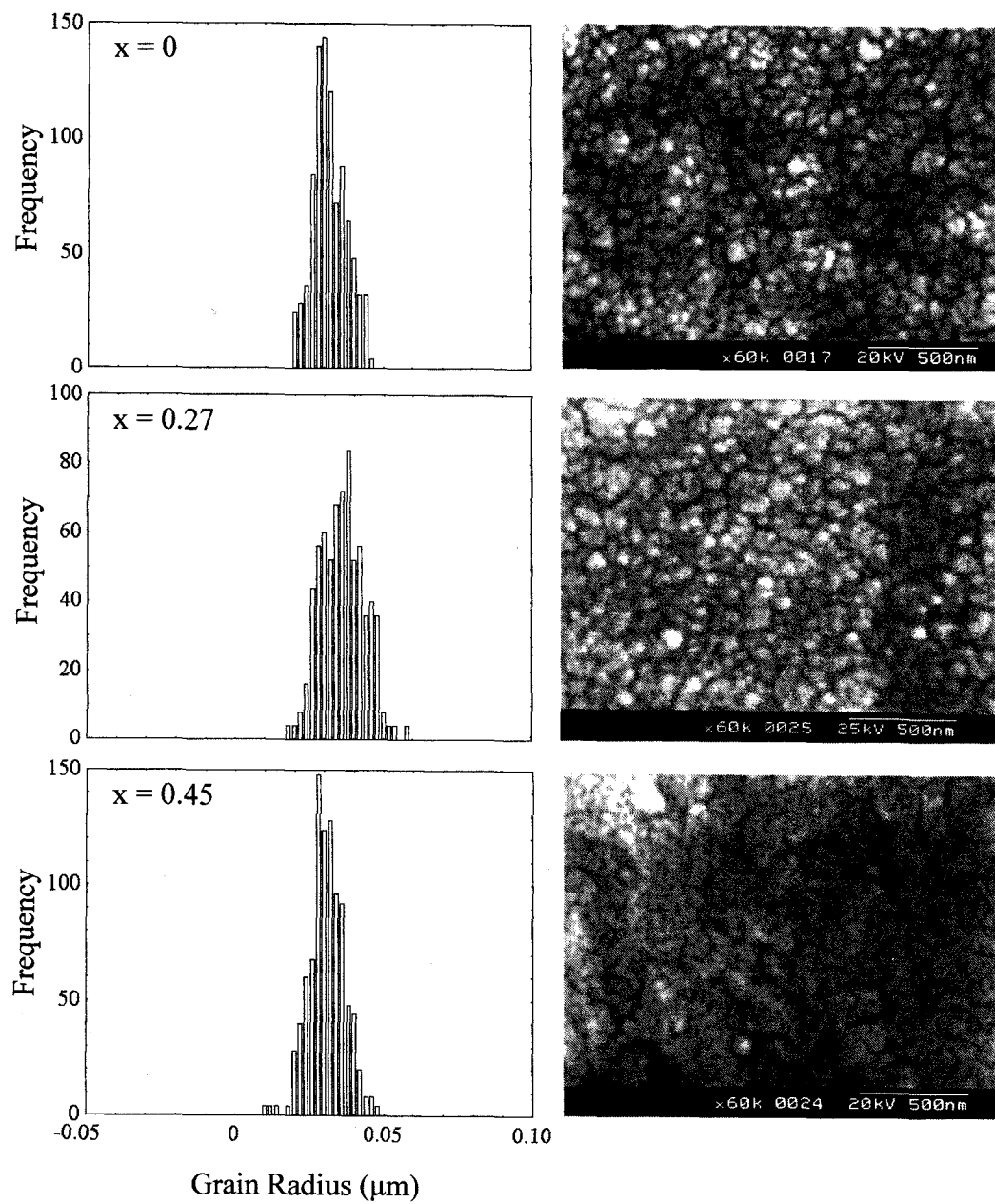


Figure 5.21a. SEM Micrographs of $\text{ZnS}_x\text{Se}_{1-x}$ Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle.

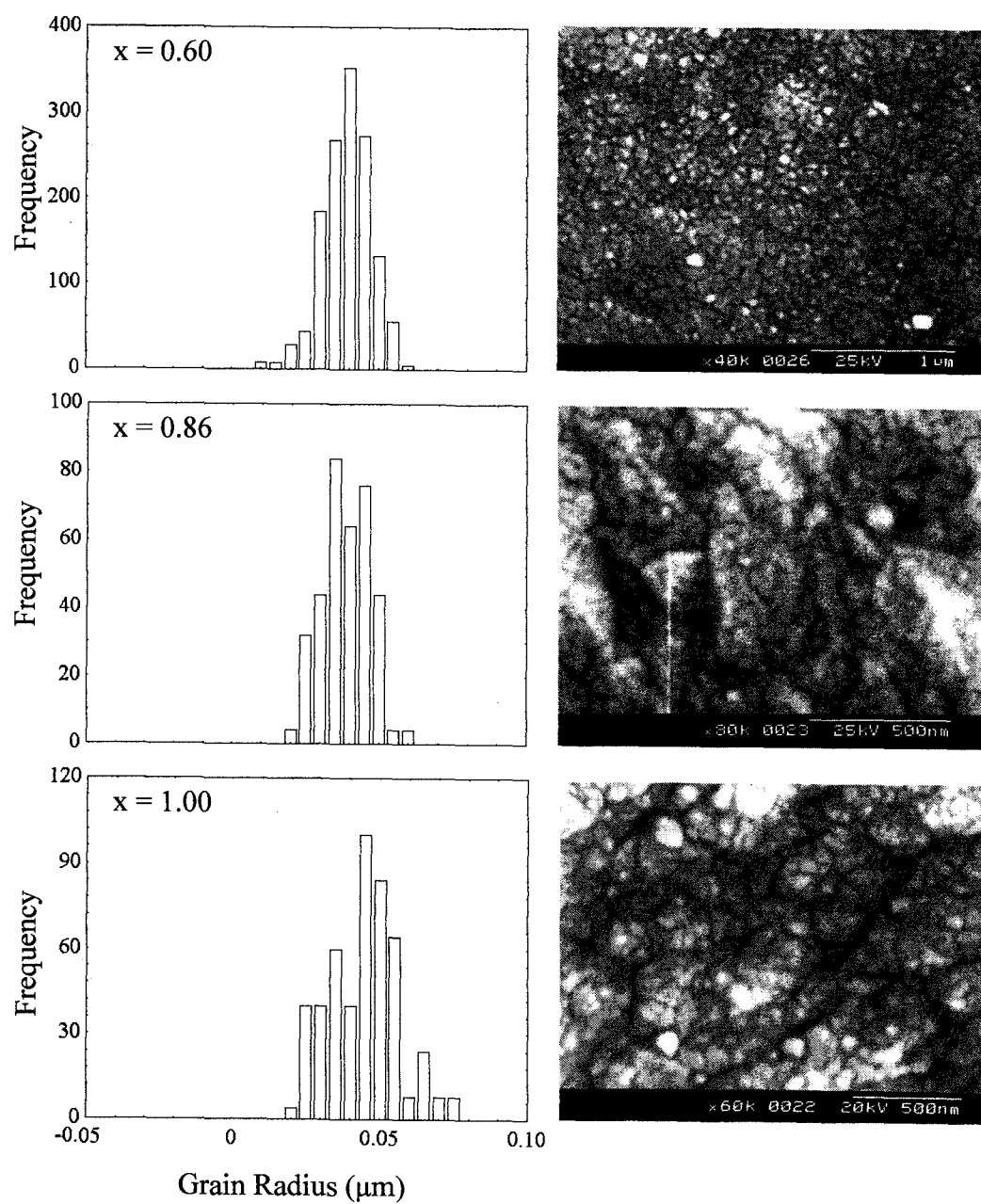


Figure 5.21b. SEM Micrographs of $\text{ZnS}_x\text{Se}_{1-x}$ Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

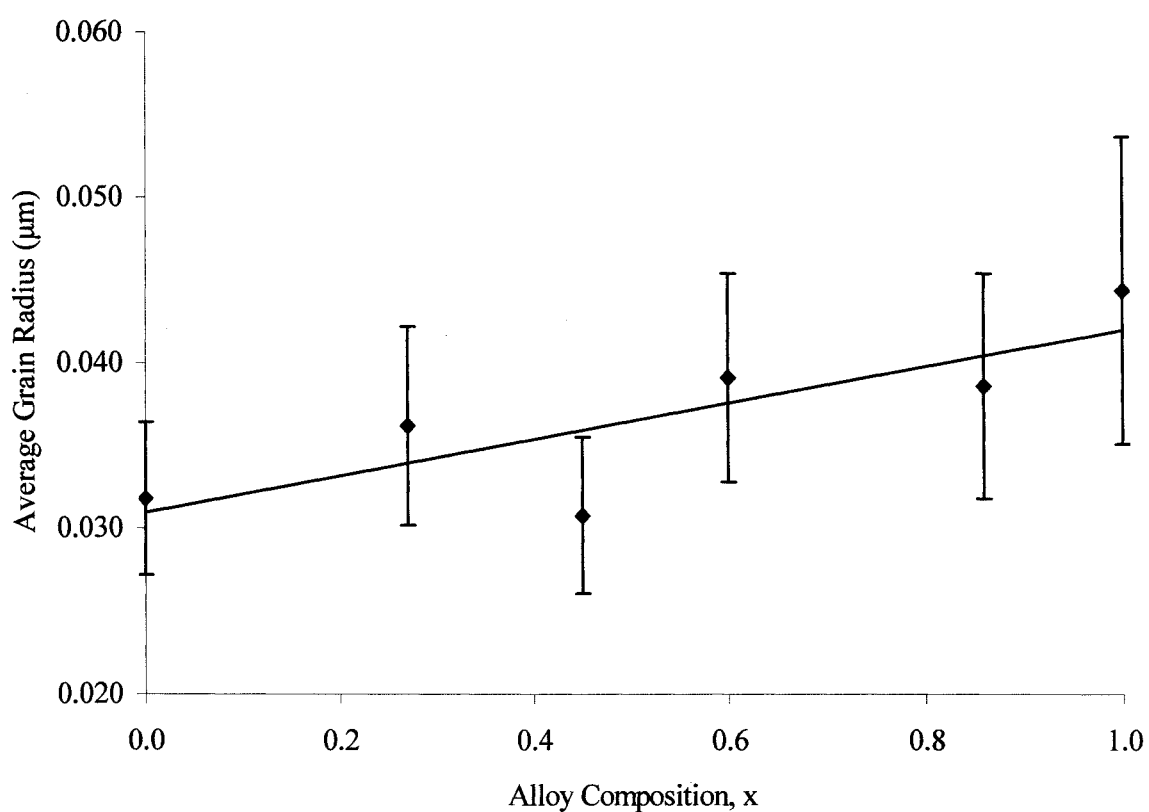


Figure 5.22. Average Grain Radius Versus Alloy Composition for $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

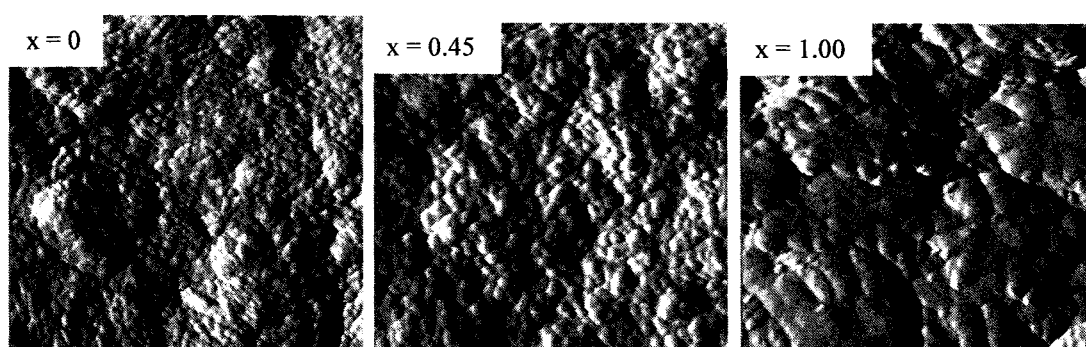


Figure 5.23. AFM Micrographs for $\text{ZnS}_x\text{Se}_{1-x}$ Deposited with
Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle
(Dimensions of each Micrograph are 1.0μm x 1.0μm).

The growth rates of the coatings were determined by recording the length of the deposition and measuring the thickness of the layers. This was achieved by ensuring some evaporant remained after deposition. Originally it was intended that a Talystep could be used to determine the layer thickness, but after initial measurements it was found that the instrument was damaging the coating. Therefore the SEM was used to directly measure the thickness of the layers. Also, where possible, the thickness of the coatings were confirmed using the interference fringes of successive minima and maxima obtained from the transmittance data [2]. The growth rate as a function of alloy composition is plotted in figure 5.24 and shows a slight decrease with increasing ZnS content. As the deposition system is set up to produce single source evaporation of $\text{ZnS}_x\text{Se}_{1-x}$, the average deposition rate, for the whole alloy system, was determined to be $0.80 \pm 0.03 \mu\text{m} \cdot \text{min}^{-1}$.

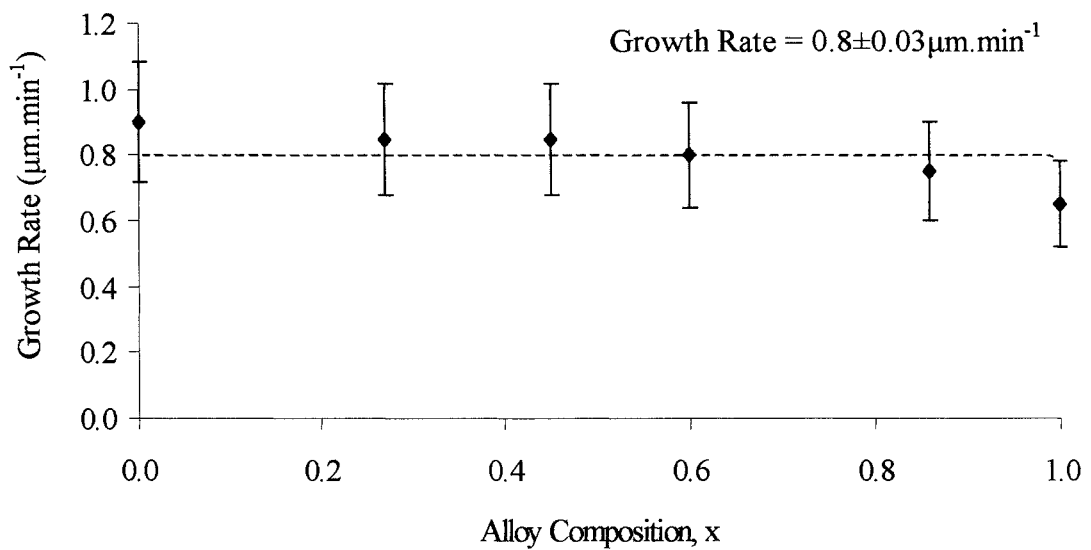


Figure 5.24. Growth Rate Versus Alloy Composition for $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle.

5.2.8 Optical Properties of $\text{ZnS}_x\text{Se}_{1-x}$ - 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle

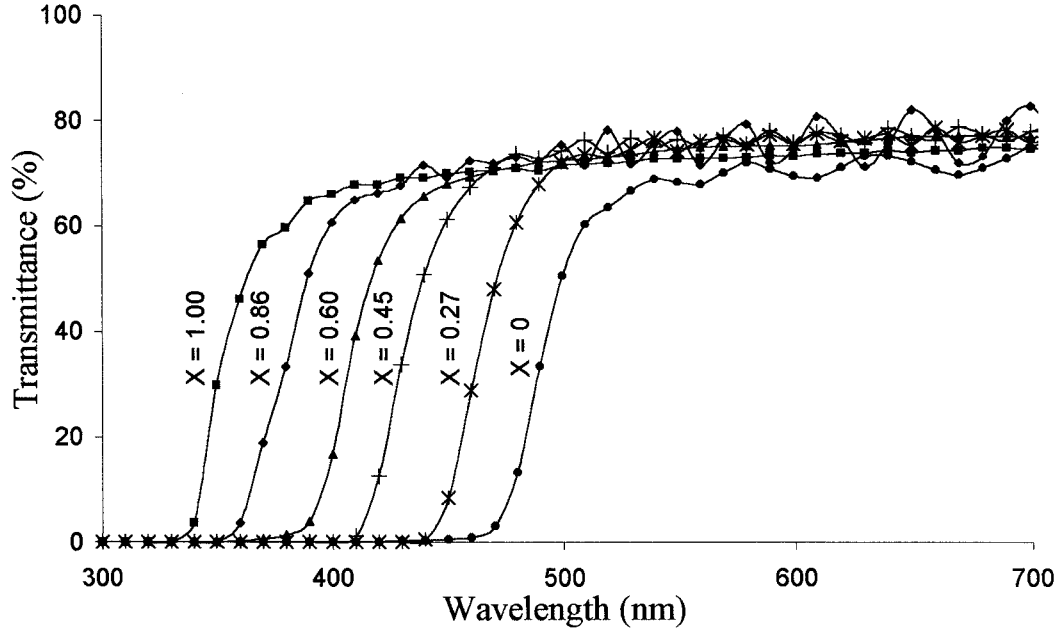


Figure 5.25. Transmittance as a Function of Wavelength for $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle.

The transmittance data of the $\text{ZnS}_x\text{Se}_{1-x}$ coatings were measured with respect to wavelength, figure 5.25. This shows a systematic shift in absorption edge with increasing ZnS content. These data were then used to plot a graph of $(\alpha h\nu)^2$ versus $h\nu$ to determine the shift in energy band gap with alloy composition, figure 5.26 (it should be noted that the energy bandgaps extrapolated from these data were taken individually from A4 diagrams). Since it is assumed that Vegards principle applies to this alloy system, the energy bandgap can be plotted against the alloy composition (obtained assuming a linear relationship between the lattice constants). Such a plot is shown in figure 5.27 and the data tabulated in 5.8. In section 3.2, the relationship between binary compounds was introduced. Equation 3.23 gives a quadratic relationship for the energy bandgap of a ternary system

$$Eg_{(x)} = \overline{Eg_{(x)}} - bx(1-x) \quad 5.7$$

which can be written as

$$Eg_{(x)} = Eg_1 + ax + bx^2 \quad 5.8$$

where b is the composition independent bowing parameter. Therefore using the data from table 5.8, the bowing parameter for the system can be calculated and for this alloy composition (at 300K)

$$Eg_{(x)} = 0.51x^2 + 0.46x + 2.64 \quad 5.9$$

Calculating the standard deviation of these data gives a bowing parameter of $0.51 \pm 0.05 \text{ eV}$. Other workers have found bowing parameters ranging from 0.46 to 0.805 eV (at 300K) for sphalerite crystal structure grown using many techniques (see table 3.1). $\text{ZnS}_x\text{Se}_{1-x}$ deposited using evaporation has produced a bowing parameter of $0.545 \pm 0.048 \text{ eV}$ [21], which allowing for errors, is in agreement with that found in this work.

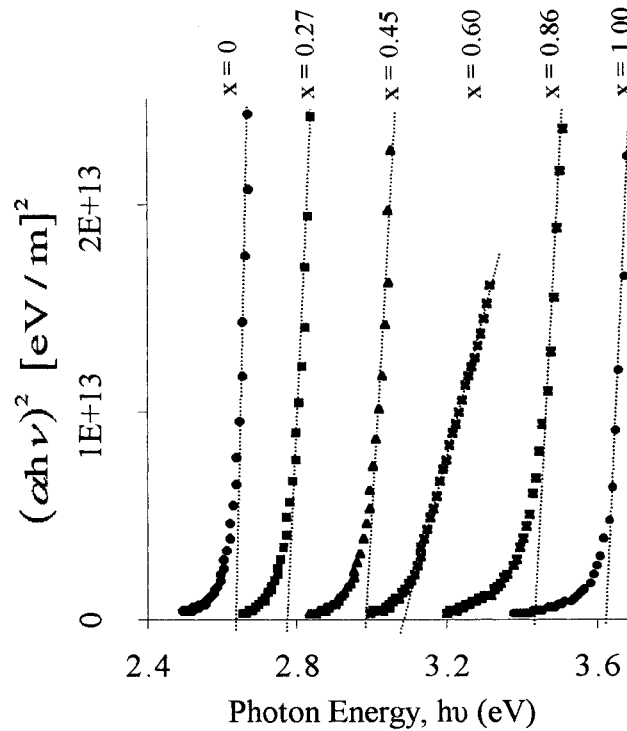


Figure 5.26. $(\alpha h\nu)^2$ as a Function of Photon Energy ($h\nu$) for $\text{ZnS}_x\text{Se}_{1-x}$ Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle.

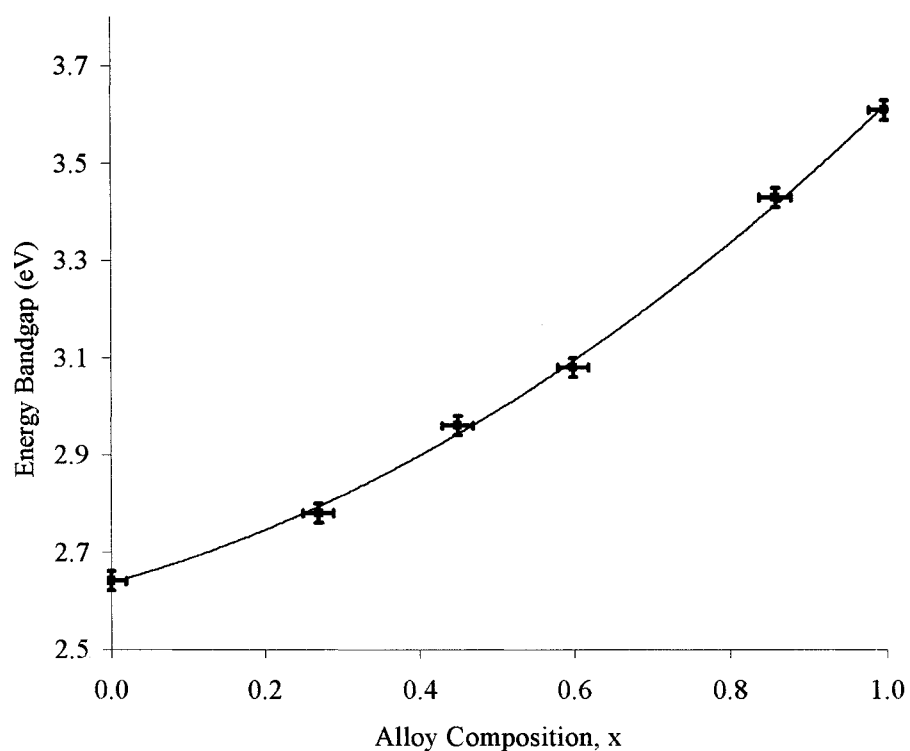


Figure 5.27. Energy Bandgap as a Function Alloy Composition for $\text{ZnS}_x\text{Se}_{1-x}$
Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

x value (± 0.02)	Energy Bandgap ($\pm 0.02\text{eV}$)
0	2.64
0.27	2.78
0.45	2.96
0.60	3.08
0.86	3.43
1.00	3.61

Table 5.8 Alloy Composition, x, and Corresponding Energy Bandgap for
 $\text{ZnS}_x\text{Se}_{1-x}$ Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle.

5.3 Optimisation of $\text{ZnS}_x\text{Se}_{1-x}$ Layers for Solar Cells

For the ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ coatings discussed thus far, no mention of electrical properties has been made. The as-deposited coatings were so resistive that a sputtered layer of Au was required to enable SEM analysis to take place (not for EDS samples). In an attempt to overcome these high resistivities problems, an investigation was undertaken to see if $\text{ZnS}_x\text{Se}_{1-x}$ could be engineered with properties that would enable use in solar cell devices. Superstrate configuration solar cells are often manufactured on a SnO_2 coated glass substrate onto which the buffer, absorber layer and finally back contacts are deposited (see figure 2.21). Since the lateral resistivity of the previous layers was so high, $\text{ZnS}_x\text{Se}_{1-x}$ was deposited onto SnO_2 coated glass substrates with the addition of Ohmic In contacts, to allow the series resistance through the layer to be measured. To reduce the $\text{ZnS}_x\text{Se}_{1-x}$ resistance, two approaches were adopted (i) an investigation into doping was undertaken and (ii) thinner layers were fabricated. All layers in this investigation were produced using the same deposition parameters as section 5.2.7 and 5.2.8.

Since p-CdTe is preferred in this solar cell configuration, due to the minority carrier length of electrons being longer than holes (as discussed in chapter 2), the $\text{ZnS}_x\text{Se}_{1-x}$ should be n-type doped. To achieve this, the cation (Zn) can be doped with a group III element or the anions (Se and S) can be n-type doped with a group VII element. In an attempt to dope both parts together, the III – VII compound AlCl_2 was used. The ZnSe and AlCl_2 were mixed by mass and added to the crucible, as described in section 5.2. Attempts were made to evaporate this mixture but problems were found with the vacuum pressure. It was found that only small amounts of AlCl_2 could be used ($< 5\%$) and when the series resistance was measured, this made no difference to the resistivity of the layers when compared to undoped layers grown using a similar approach.

5.3.1 SnO_2 / $\text{ZnS}_x\text{Se}_{1-x}$ at 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle

To produce thinner $\text{ZnS}_x\text{Se}_{1-x}$ layers, the growth rate data from figure 5.28 was taken into consideration. Three different structures were grown, ZnSe , $\text{ZnS}_{0.50}\text{Se}_{0.50}$ and ZnS (on SnO_2 / glass) assuming a growth rate of $0.8\mu\text{m}\cdot\text{min}^{-1}$ (see section 5.2.7.).

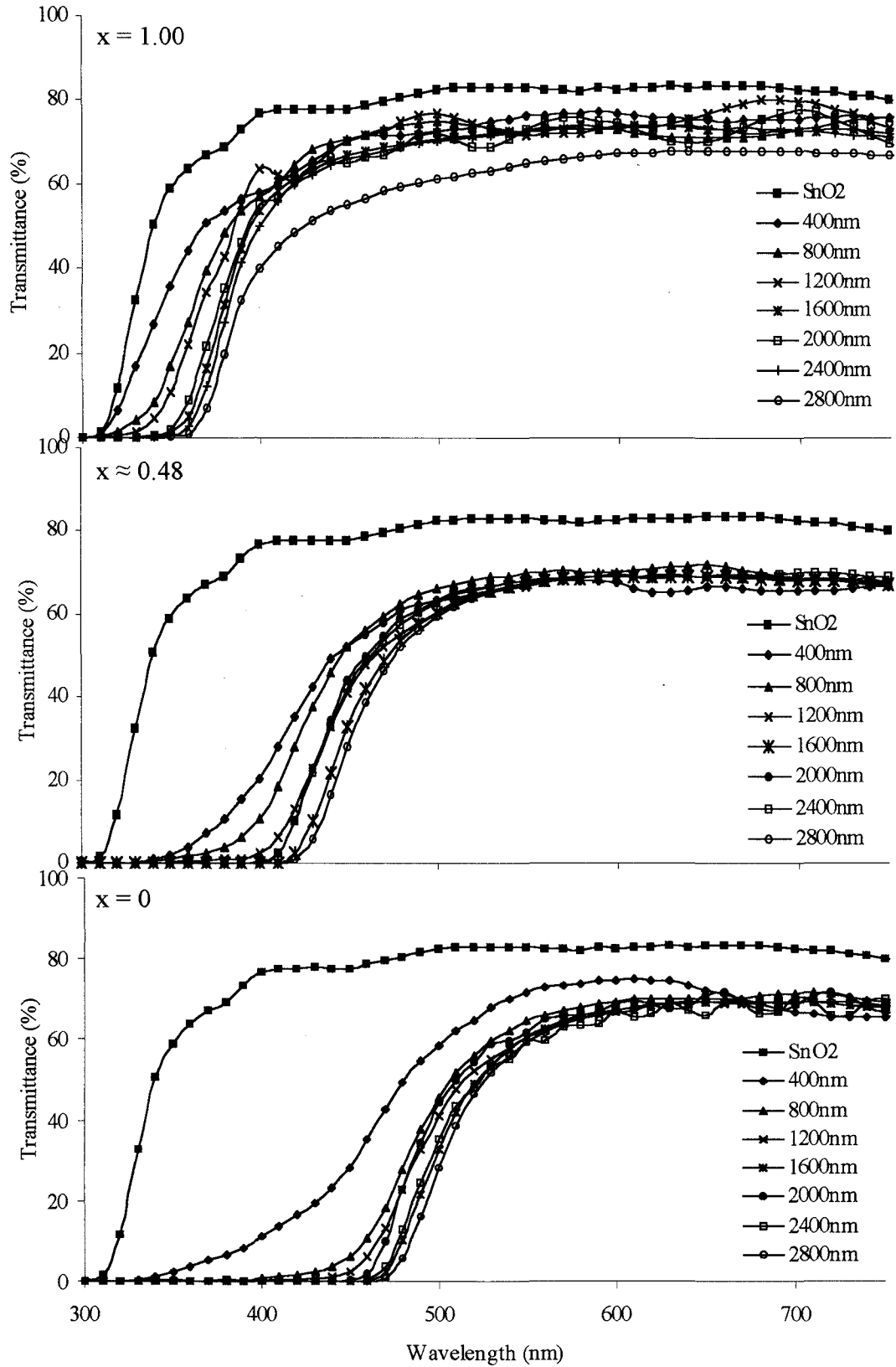


Figure 5.28. Transmittance as a Function of Wavelength for $\text{SnO}_2/\text{ZnSn}_x\text{Se}_{1-x}$
 Deposited with Parameters 11mm / T_{source} 600°C / T_{sub} 200°C / Baffle
 and Varying Layer Thickness (Insert: Nominal Thickness of $\text{ZnSn}_x\text{Se}_{1-x}$ Layers).

The transmittance versus wavelength curves for these three structures with varying nominal thicknesses are shown in figure 5.28. The thickness is described as nominal as they were not measured and assume a similar uniform growth rate across the alloy range.

The alloy composition of the $\text{ZnS}_{0.50}\text{Se}_{0.50}$ layers was determined from the XRD data and an average value of $x \approx 0.48$ was found. It was difficult to be precise about the alloy composition of the thinner layers, as the intensity of the diffraction peaks were lower and the peaks from the SnO_2 substrate became more distinct, distorting the results. Grouped XRD data showing this, figure 5.29, illustrates the growth in the SnO_2 phases in respect to the ZnSSe coating. The diffraction data, figure 5.30, of the SnO_2 coated glass substrate is shown to illustrate the structure before coating.

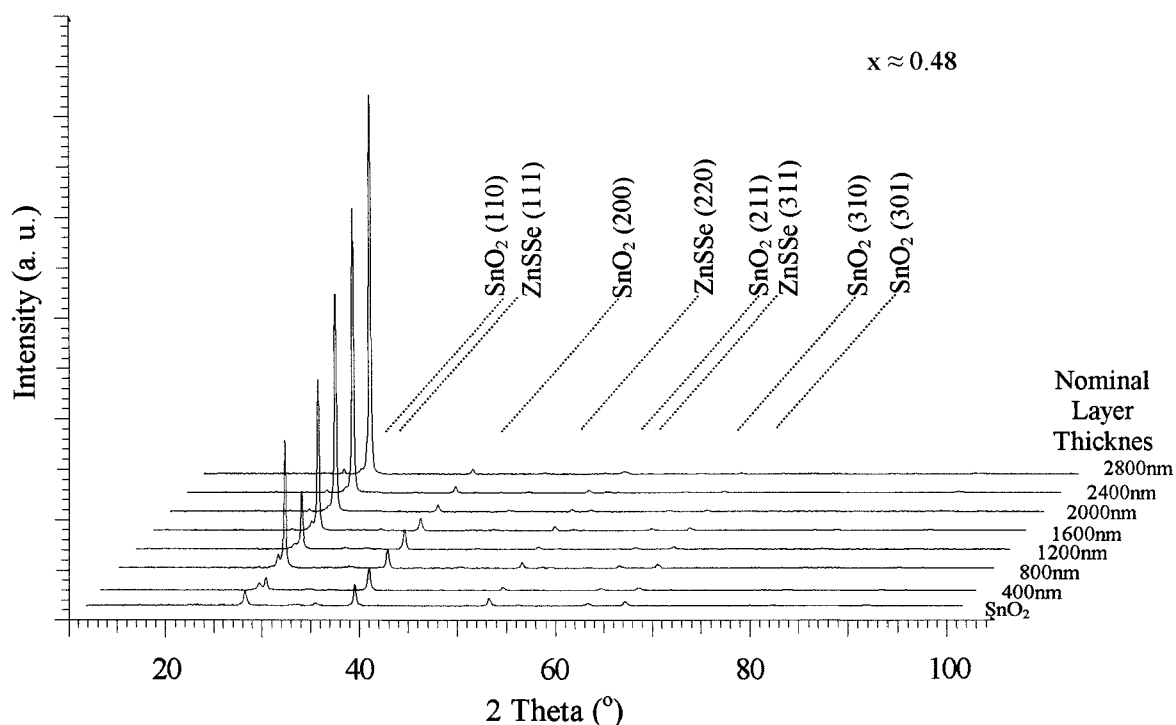


Figure 5.29. Grouped XRD Data of $\text{SnO}_2 / \text{ZnS}_x\text{Se}_{1-x}$ with Varying Layer Thickness
Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle.

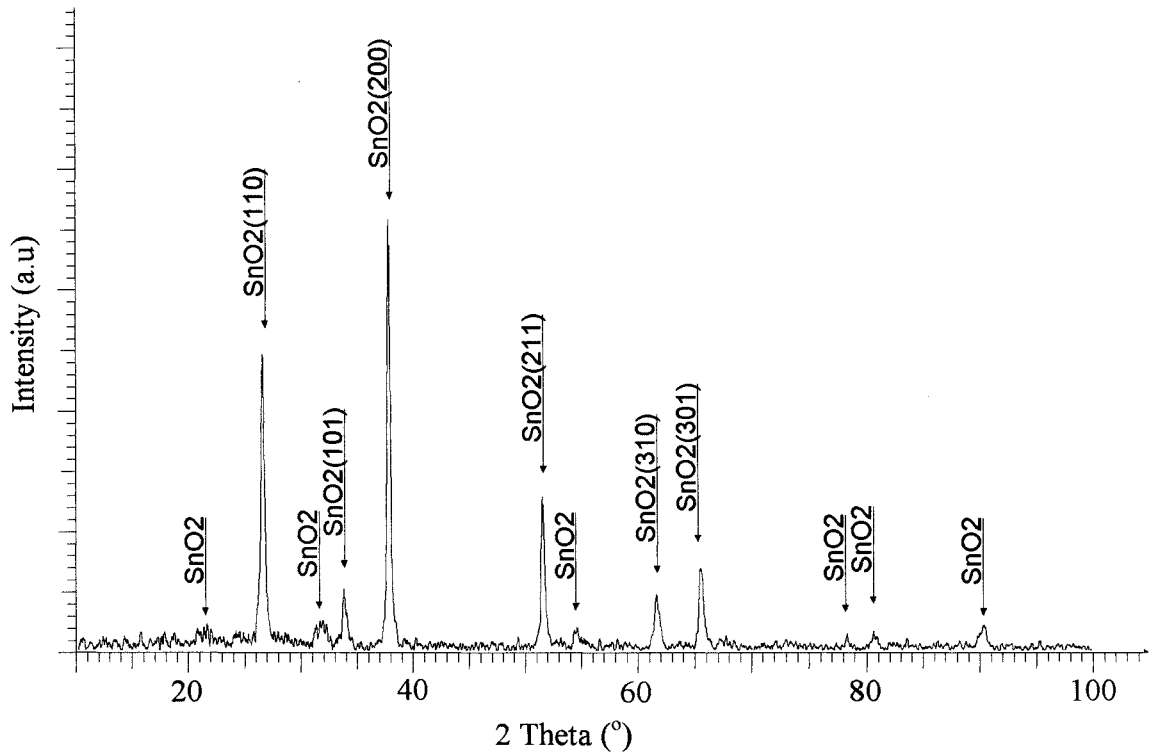


Figure 5.30. XRD Data of SnO₂ Coated Glass Substrate.

Indium contacts were deposited onto SnO₂ / ZnS_xSe_{1-x} layers and the series resistance was measured. This was achieved by placing one spring probe from the testing rig on the uncoated SnO₂ and the other on the indium contact. Using the IV apparatus described in section 4.3.4.1, the series resistance was calculated. Conventionally, series resistance would be discussed in terms of Ohms, but in this case, the units are $\Omega \cdot \text{cm}^{-2}$ to allow for the In contacts sizes. The sheet resistance of the SnO₂ layers was measured using the four probe apparatus and found to be $12.5 \Omega \cdot \square^{-1}$, which is comparable with that used by other workers for high efficiency (>10%) CdS / CdTe devices ($10 \Omega \cdot \square^{-1}$ [22], $8\text{-}10 \Omega \cdot \square^{-1}$ [23] and $10 \Omega \cdot \square^{-1}$ [24]). The calculated series resistance versus layer thickness are plotted in figure 5.31. The lowest resistance measured was $58 \Omega \cdot \text{cm}^{-2}$, which is still much larger than required when producing solar cells (i.e. a few Ohms) [25]. However, the resistance of the thicker layers is much larger with a value $> 1000 \text{ Ohms} \cdot \text{cm}^{-2}$ for the layer $2.8 \mu\text{m}$ thick.

Therefore, using thinner layers has reduced the series resistance of the as-deposited films.

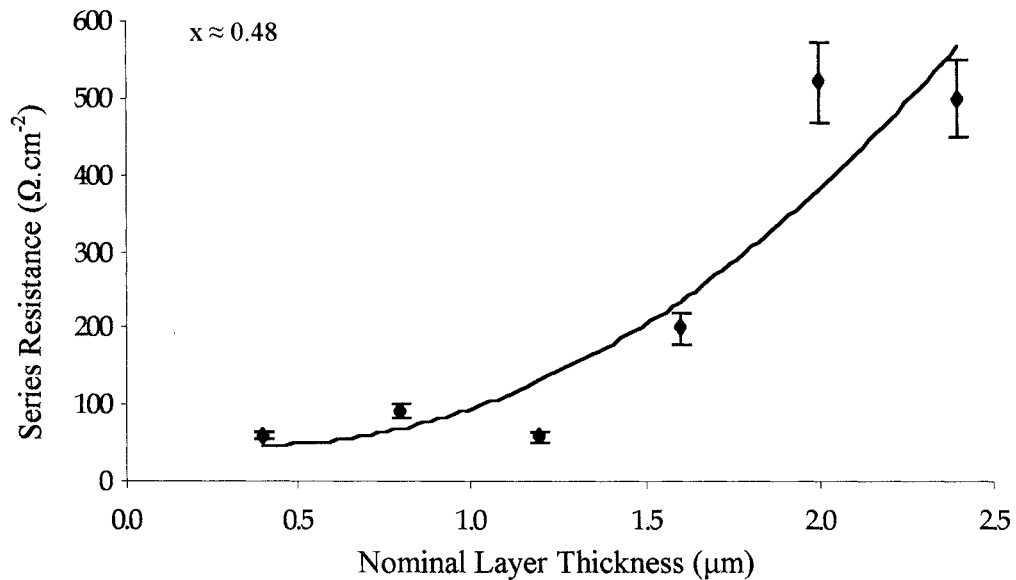


Figure 5.31. Series Resistance of $\text{SnO}_2 / \text{ZnS}_x\text{Se}_{1-x}$ Versus Nominal Layer Thickness Deposited with Parameters 11mm / $T_{\text{source}} 600^\circ\text{C}$ / $T_{\text{sub}} 200^\circ\text{C}$ / Baffle.

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Chapter Six

CdTe Layers

6.1 Preferred Growth Conditions and Plant Set-Up

It was intended from the outset that the growth of the absorber layers should, if at all possible, take place in the same chamber as the buffer layers and without breaking vacuum. This was intended to reduce the risk of interface contamination, due to accidental impurity incorporation when re-charging deposition plant between layers.

The mechanical set-up of the source and substrate for the buffer layers were determined in chapter 5 and therefore the absorber layer source positioning was also governed by this. As the optimum buffer layer distance was 11mm, this did not leave much room for the positioning of the absorber layer source. It was found that the best physical set-up was to also position the absorber layer source-substrate distance at 11mm. This left the only deposition parameters to be altered as the source and substrate temperatures.

The properties of an ideal polycrystalline absorber layer were discussed in chapter 2. Since some of these characteristics have already been addressed by the selection of CdTe, such as the preferred energy bandgap ($\sim 1.4\text{eV}$) and the direct nature of the bandgap, the remaining properties that need to be considered in the search for a heterojunction partner for $\text{ZnS}_x\text{Se}_{1-x}$ are:

- (i) The material should be p-type due to the minority carrier diffusion length of electrons and to form a pn junction with the n- $\text{ZnS}_x\text{Se}_{1-x}$ buffers.
- (ii) Large, densely packed columnar grains are desired, which reduce the losses due to grain boundary recombination.
- (iii) The resistivity should be sufficiently low to avoid series resistance problems.

6.2 Optimisation of As-Deposited CdTe

An investigation was commenced in an attempt to find the best set of parameters that yield an optimum coating for partnering n-ZnS_xSe_{1-x}. The CdTe layers were produced using a similar approach to the ZnS_xSe_{1-x} layers of chapter 5. CdTe was once again deposited using single source evaporation, with an evaporant (of purity of 99.999% purchased from Johnson Matthey) placed in a bottle shaped quartz crucible. Quartz wool was also used to prevent spattering and the tantalum heating element was purchased from R.D. Mathis Company. The CdTe and crucible were outgassed with temperature of ~ 200°C. For all CdTe layers deposited, the material characterisations of section 5.1 were carried out.

According to the literature, a source temperature greater than 450°C is required to evaporate CdTe in a vacuum of 10⁻⁴ Torr [1], therefore the first attempts to find the optimum deposition parameters were with a source temperature of 500°C. Substrate temperatures from 100 to 600°C were used in this initial investigation and the CdTe was deposited onto soda lime glass microscope slides, cleaned as described in chapter 5. Prior to the start of the deposition, the vacuum pressure was lower than 5x10⁻⁶ mbar. During deposition, the vacuum pressure increased but at all times was kept below 10⁻⁴ mbar. As discussed in chapter 3, most CdTe based solar cells use a post deposition CdCl₂ treatment to enhance the junction properties. Workers have found that the CdCl₂ treatment facilitates grain growth of the as deposited CdTe [2,3]. Therefore, the desired topology was that of (i) large as-grown grains or (ii) densely packed grains which would give rise to grain growth after the post deposition treatment, both of which would facilitate type conversion of the CdTe [4].

The SEM micrographs of four as deposited coatings are shown in figure 6.1. These layers were produced with a source temperature of 500°C and varying substrate temperatures as indicated. The coatings of the 200 and 450°C depositions appear to be uniform and free from pinholes but not the morphology associated with good CdTe layers. The micrographs of the 250 and 350°C samples show that the coating is not uniform and there are large discontinuities in the layer. Problems were encountered with substrate temperatures above 500°C culminating in very poor coating adhesion at 600°C.

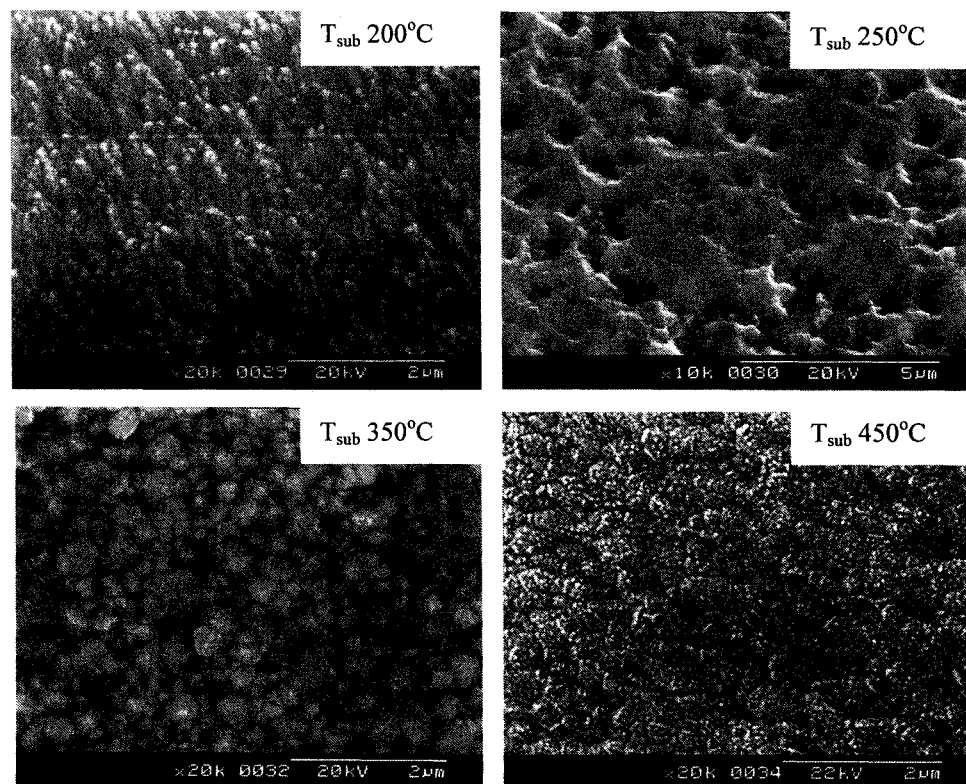


Figure 6.1. SEM Micrographs of As Deposited CdTe with Source Temperature of 500°C and Varying Substrate Temperatures as Indicated.

6.2.1 Structural Properties of As-Deposited CdTe

In an attempt to overcome the adhesion problems and surface irregularities encountered with the previous coatings, the source temperature was increased to 600°C and a tantalum baffle was placed between the source and substrate. As can be seen in the micrographs of figure 6.2, the coatings appear to be uniform and free of pinholes (confirmed with lower SEM magnification). These images show how the topography of the 200 and 250°C samples seem similar. At 300°C, the grains appear to be forming islands, whereas at 350°C the grains have apparently coalesced. However, at even higher temperatures, these “groupings” have lost their structure and the boundaries between neighbouring islands are less clear. To further investigate the structure of these layers, XRD data was taken and the diffraction patterns for three of the five films are shown in figure 6.3 (the pattern for the 350°C is shown in figure 6.10). At first inspection, the patterns for the lower substrate temperatures appear to show both sphalerite (c) and wurtzite (h) phases, whereas at high temperatures, only the sphalerite structure prevails. The properties of ball milled CdS and CdSe and their structural aspects have been investigated by other workers [5]. In this study it was found that for both alloys, the unmilled or lightly milled compounds were wurtzite, whereas after milling, the phases appeared to be of a cubic (sphalerite) nature. It was also found that after heat treatment of the compounds (at temperature greater than 400°C) they reverted back to the wurtzite phase. It was therefore postulated that the milling process had introduced stacking disorders through dislocation movement, which were corrected by the heat treatment. It was therefore concluded that the cubic appearance of the phases was due to randomisation rather than phase changes. If this supposition can be applied to the CdTe in this work, then the lower substrate depositions could be classified showing randomisation. However, the higher substrate temperatures would allow formation of the more natural sphalerite phase for this method of layer fabrication. This was confirmed by post deposition heat treatment of the as deposited layers (see section 6.3) in which only the cubic phase propagated.

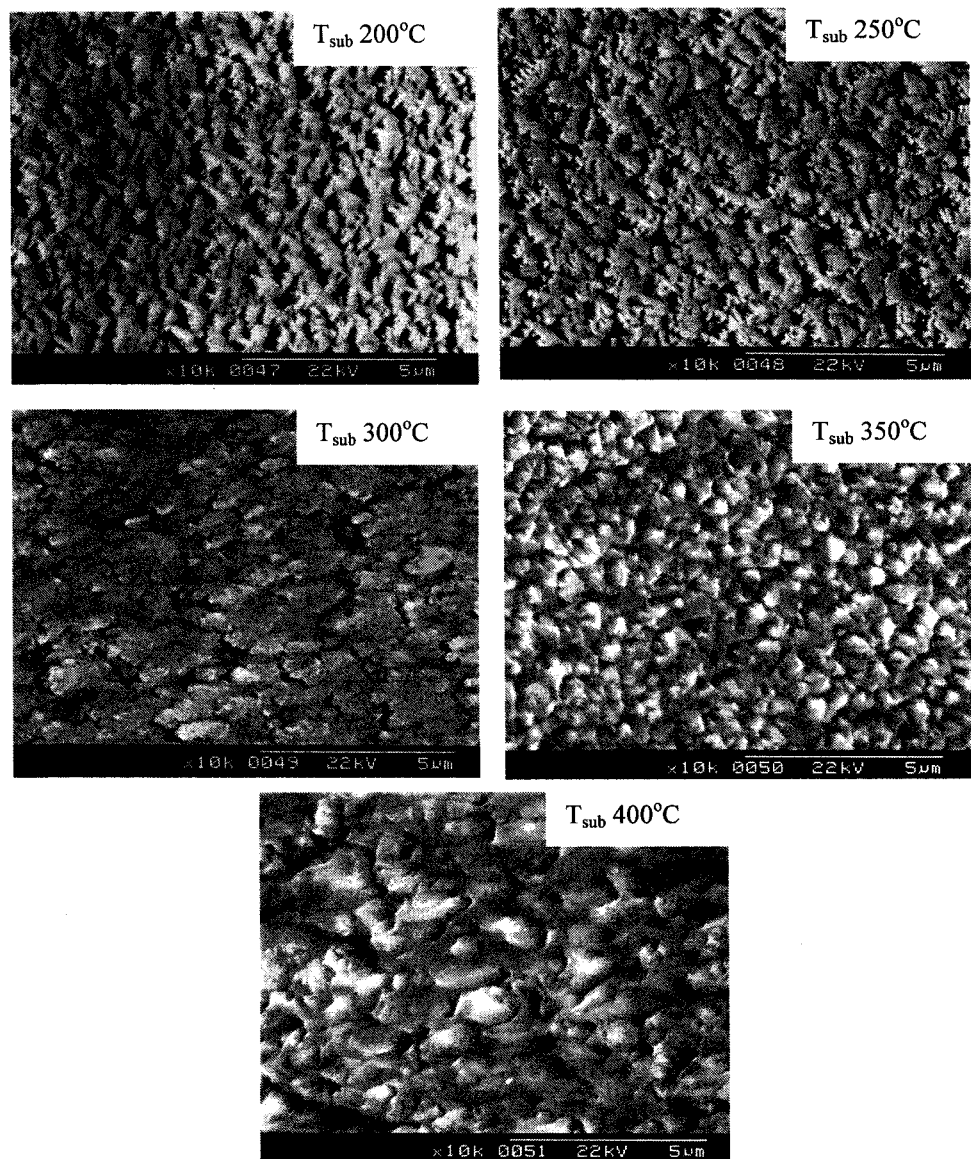


Figure 6.2. SEM Micrographs of As Deposited CdTe with Source Temperature of 600°C and Varying Substrate Temperatures.

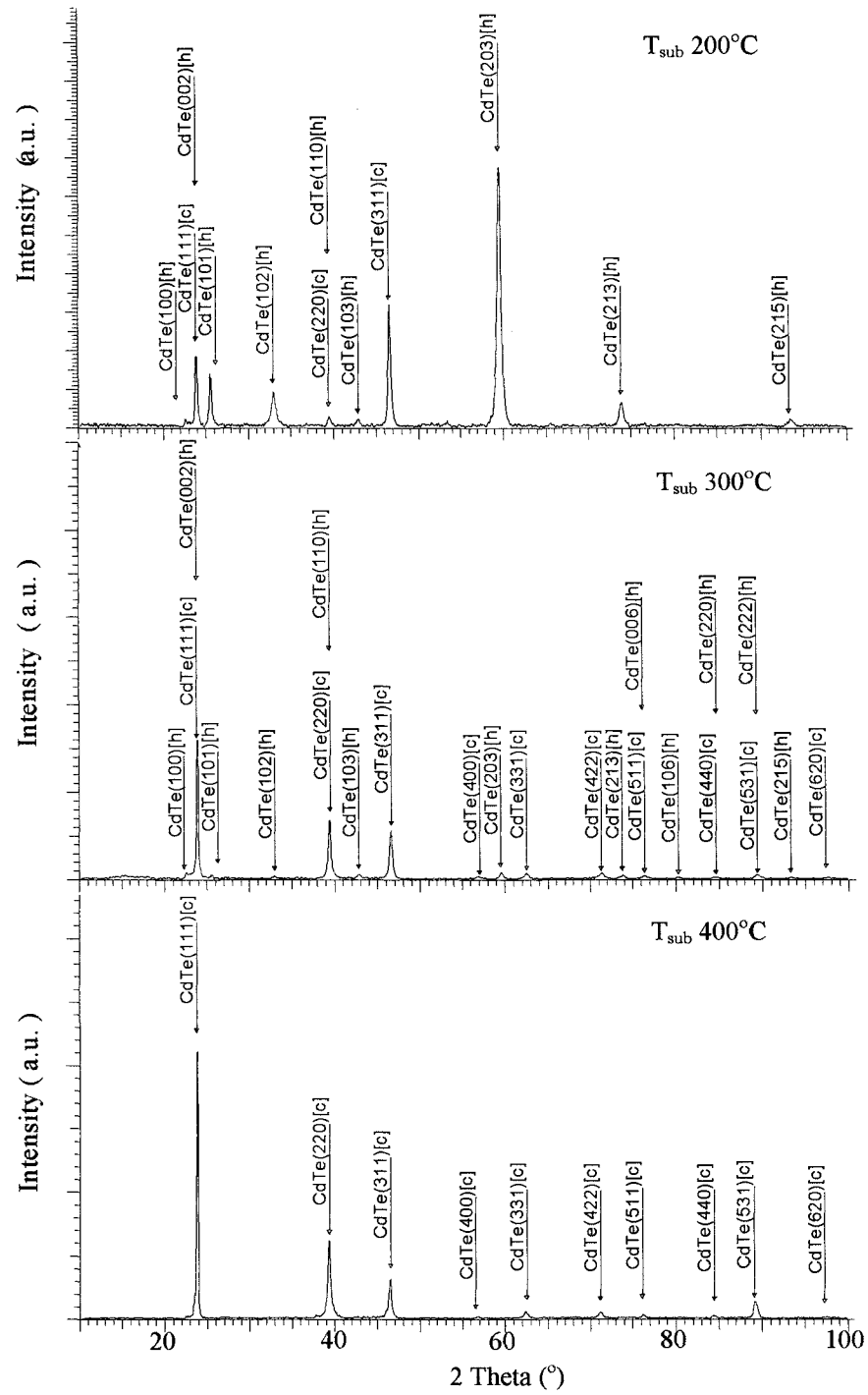


Figure 6.3. XRD Data of As Deposited CdTe with Source Temperature of 600°C and Varying Substrate Temperatures.

(note: [h] = hexagonal or wurtzite and [c] = cubic or sphalerite phases)

To further investigate the X-ray diffraction data, the FWHM of the cubic (111) and (311) peaks were plotted as a function of substrate temperature, figure 6.4. The data for the (111) peak indicates a general narrowing of the half width, confirmed by the XRD in an increase in intensity as compared with the other phases. Conversely for the lower temperatures, the (311) peak shows a widening in the half width before narrowing at higher temperatures. Since these data cover a temperature range in which the cubic and hexagonal phases are present, then the lower temperature data may not be valid. Therefore, from 300°C, where the diffraction pattern is almost entirely of a cubic nature, the general trend for both the (111) and (311) peaks is a narrowing of the FWHM with increasing substrate temperature.

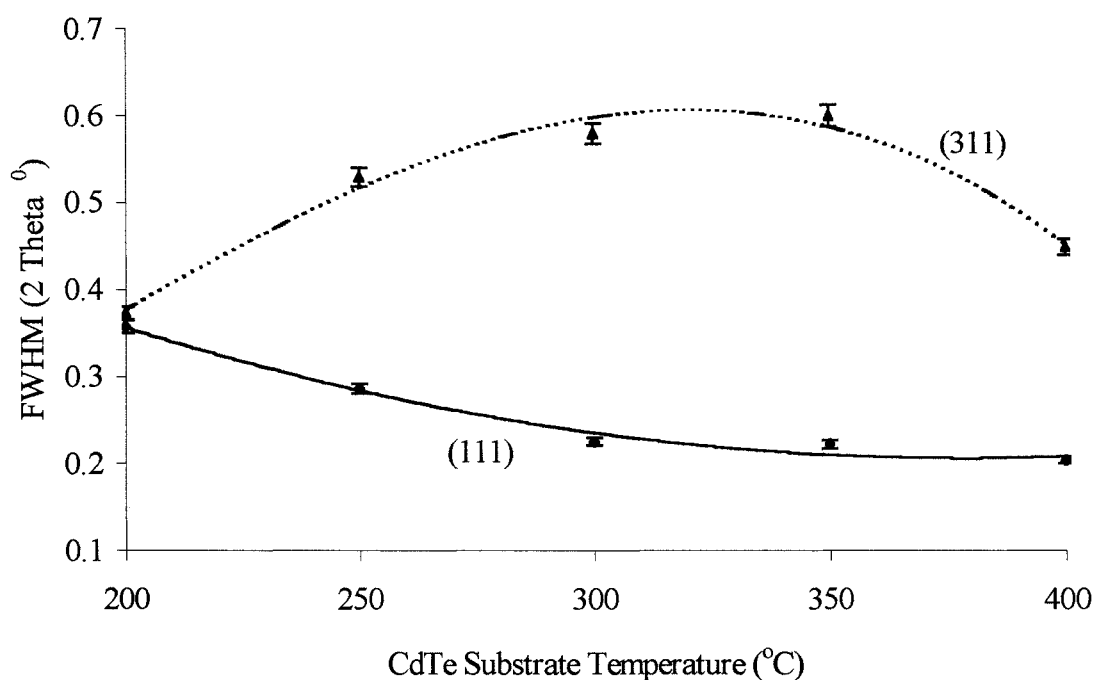


Figure 6.4. FWHM Versus Substrate Temperatures Determined from XRD Data for As Deposited CdTe with Source Temperature of 600°C

In a further attempt to investigate the material trends of the as deposited CdTe, the crystallite size was determined from the X-ray diffraction data using the Scherrer technique, as described in chapter 5. The (111) peak shows an increase in crystallite

size with substrate temperature and where, if ignoring the lower temperature data, the (311) peak also shows an increase in size with increasing temperature.

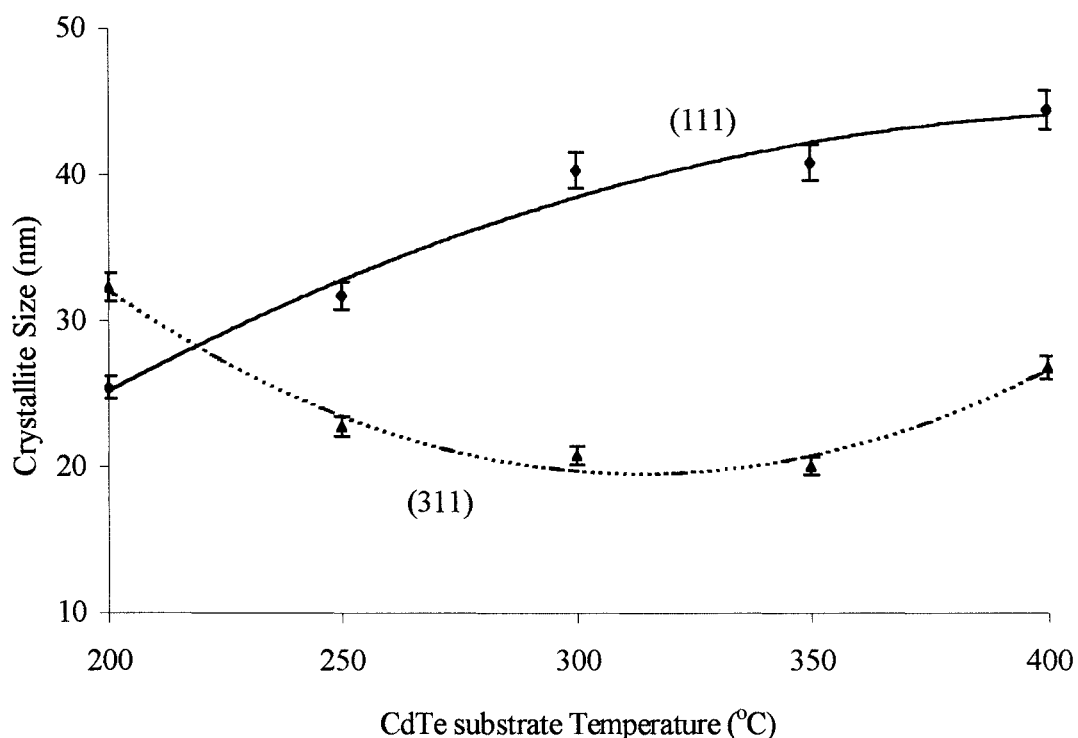


Figure 6.5. Crystallite Size Versus Substrate Temperatures Determined from XRD Data for As Deposited CdTe with Source Temperature of 600°C

The growth rate of the CdTe layers for various substrate temperatures and a source temperature of 600°C were determined, a plot of which is shown in figure 6.6. With substrate temperatures up to approximately 400°C, the growth rate is generally constant and was determined to be $1.62 \pm 0.04 \mu\text{m} \cdot \text{min}^{-1}$. A lower growth rate was found above 400°C and there was no coating adhesion at substrate temperatures above 600°C. These trends would indicate that only the supply of material appears to affect the coating thickness below 400°C. However, at higher temperatures, the coating cannot stick to the substrate and re-evaporation of the CdTe is taking place.

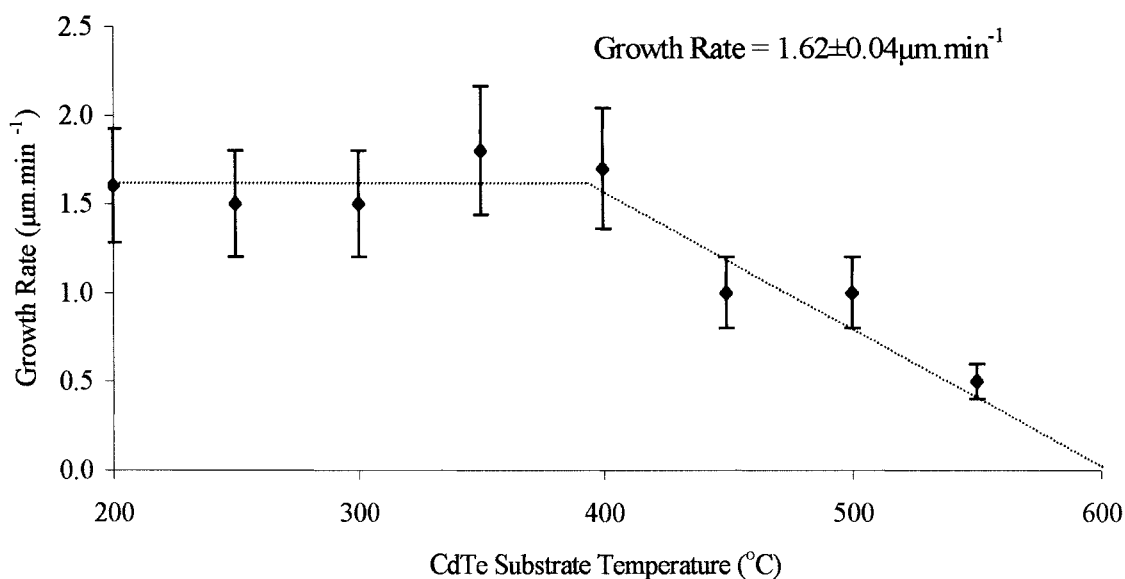


Figure 6.6. Growth Rate Versus Substrate Temperature for As Deposited CdTe Produced with a Source Temperature of 600°C

6.3 Optimisation of CdCl₂ Treatment

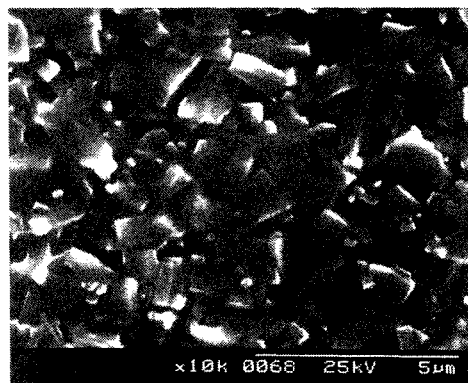
The CdCl₂ in this investigation was applied in the form of a post deposition dip [6]. The granular CdCl₂ was added to methanol until a saturated solution was obtained. This solution was then further diluted to reduce the CdCl₂ concentration (i.e. 10% solution equates to 90% methanol / 10% saturated CdCl₂ and methanol). An anneal in air then followed at a temperature of approximately 400°C, following a method used by other workers [7,8].

Initial investigations found that the selection of dip solution, annealing time and temperature were critical in achieving CdTe layers approaching PV quality [9]. The SEM images of some treated layers are shown in figure 6.7. All layers were initially deposited using the same parameters, namely a source temperature of 600°C and a substrate temperature of 350°C. The micrographs for figures 6.7a and 6.7b show similar trends in which the CdCl₂ dip does not seem to be strong enough to facilitate complete grain growth, and the topology has changed due to the air anneal. The topology of the micrograph of figure 6.7c shows a layer that has undergone rigorous structural changes. This layer was produced with the same as-deposited properties as figures 6.7a and 6.7b but a stronger solution (in terms of CdCl₂ concentration) and longer dip time were used. In addition, the annealing time was for 40 minutes. The

(a)
CdCl₂ Treatment
Dip in 10% Solution for 30 seconds
Anneal for 30 minutes at 440°C



(b)
CdCl₂ Treatment
Dip in 10% Solution for 3 Minutes
Anneal for 20 minutes at 440°C



(c)
CdCl₂ Treatment
Dip in 50% Solution for 3 Minutes
Anneal for 40 minutes at 440°C

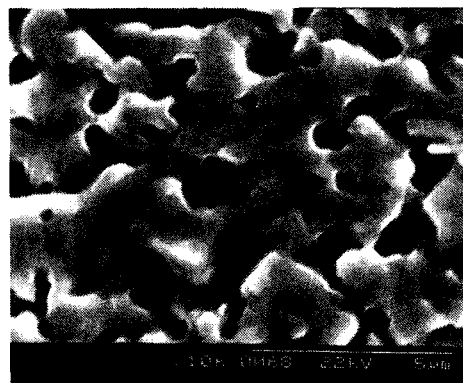


Figure 6.7. SEM Micrographs of CdCl₂ Treated CdTe
with Various Treatment Conditions
(initial CdTe deposition $T_{\text{sub}} = 350^{\circ}\text{C}$ and $T_{\text{source}} = 600^{\circ}\text{C}$)

combination of these three elements appears to be too vigorous and has drastically altered the morphology of the CdTe layer. The XRD data for two of these layers are shown in figure 6.8. The CdTe has a cubic phase but there is an incorporation of CdTeO₃, which is more pronounced with the more concentrated solution and longer dip and annealing time.

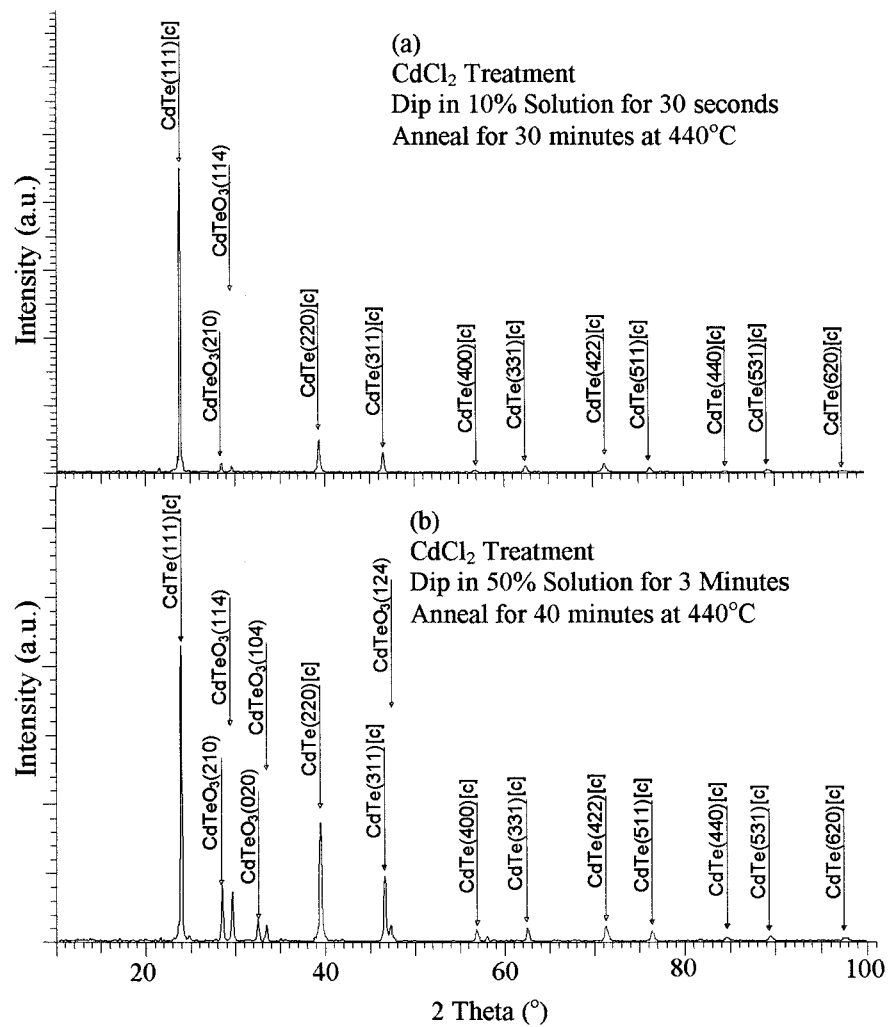


Figure 6.8. XRD Data of CdCl₂ Treated CdTe with Various Treatment Conditions.
(initial CdTe deposition $T_{\text{sub}} = 350^{\circ}\text{C}$ and $T_{\text{source}} = 600^{\circ}\text{C}$)

6.3.1 Structural Properties of CdCl₂ Treated CdTe

During initial investigations into determining the best fabrication parameters for obtaining CdTe for solar cells, the optimum CdTe deposition parameters, in terms of morphology and structure, were concluded be T_{source} 600°C and T_{sub} 350°C. The SEM micrographs of figure 6.9 show the as-deposited CdTe (figure 6.9a) and post deposition treated layers (figures 6.9b, to 6.9d). These images were all taken with the same SEM magnification and show that an increase in grain size has been realised. This culminated in the largest grain growth with a post deposition treatment of:

- (i) Solution, 50% CdCl₂ / methanol
- (ii) Dip for 1 minute
- (iii) Anneal in a furnace in air for 20 minutes

The topological changes observed in the SEM images were once again examined by the analysis software described in section 5.2.1. This software allows a Rayleigh distribution fit to the histograms given by the function [10]

$$f(r) = ar \exp(-br^2) \quad 6.1.$$

where r is the grain radius, a and b are constants (values of which are produced by the programme). The average grain radius can be determined using

$$\bar{r} = \frac{\sqrt{\pi}}{2b^{1/2}} \quad 6.2.$$

The error in the grain size was taken from the grain radius deviation and is displayed in table 6.1. The Rayleigh fit of the histogram for the optimised treatment (figure 6.9d) is comparable with data published by [11] for the grain structure of CSS deposited CdTe after CdCl₂ treatment.

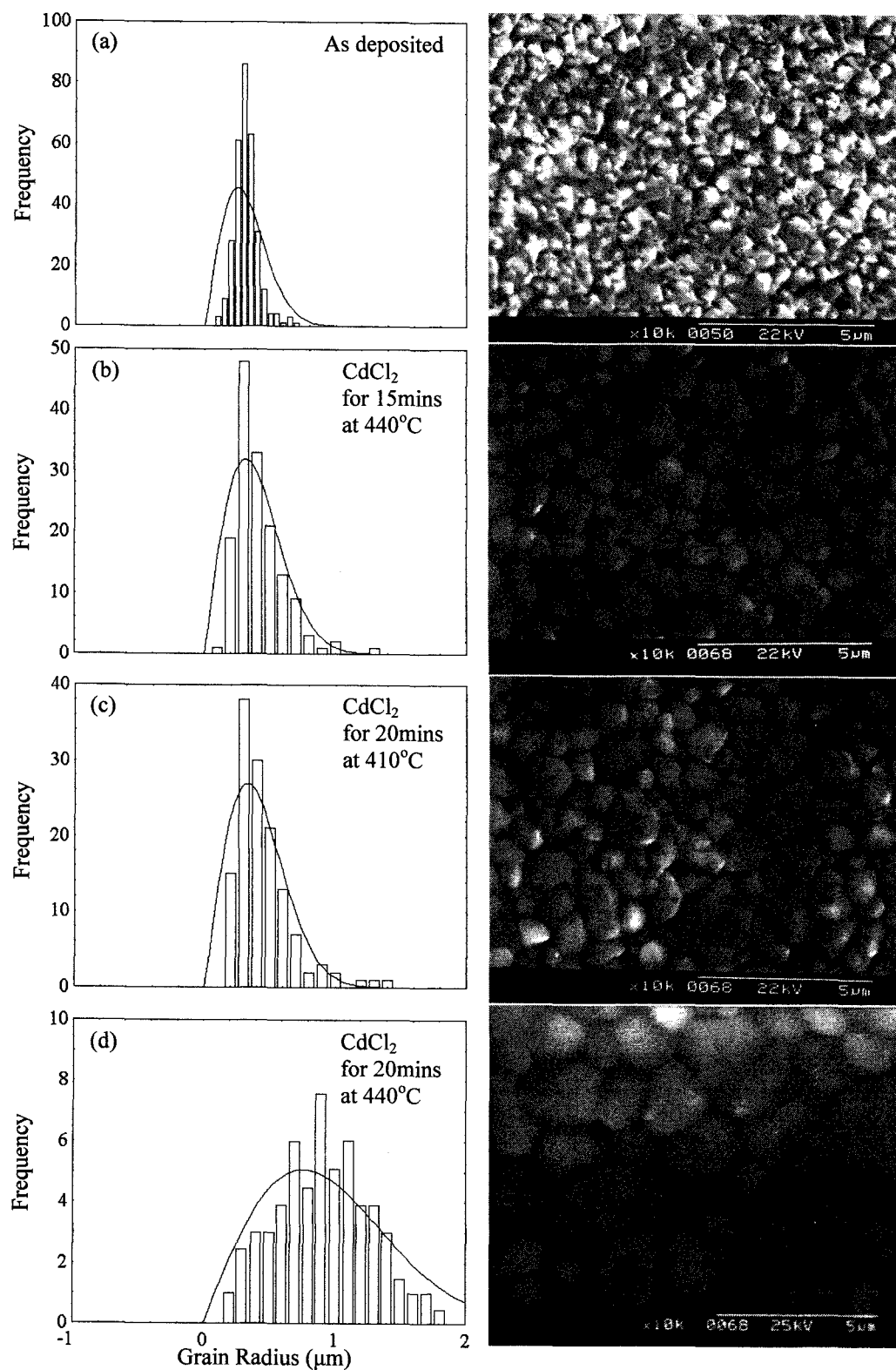


Figure 6.9. Grain Histograms and SEM Micrographs of As Deposited and CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Varying Annealing Temperatures and Times.

Layer	Average Grain Radius (μm)
As Deposited CdTe (T_{sub} 350°C)	0.312 ± 0.067
CdCl ₂ for 15 mins at 440°C	0.394 ± 0.139
CdCl ₂ for 20 mins at 410°C	0.411 ± 0.155
CdCl ₂ for 20 mins at 440°C	0.958 ± 0.271

Table 6.1. Average Grain Radius Determined from Histograms of As Deposited and CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Varying Annealing Temperatures and Times.

The X-ray diffraction data for the as-deposited CdTe and post deposition treated layers (for 20 minutes) are shown in figure 6.10. These data show the as-deposited layers (figure 6.10a) have an entirely cubic phase and large (111) peak. The treated layers (6.10b and 6.10c) however, show a relative reduction in (111) intensity and a general increase in the (220) and (311) planes, which has also been observed by other workers after annealing electrodeposited CdTe [12, 13].

To further investigate the phases of the XRD data, the texture coefficient was calculated using equation 5.5. Table 6.2 lists the calculated texture coefficients of the as-deposited and treated layers. Examining the standard deviation data (determined using equation 5.6) of table 6.2 shows that for all layers there is some preferred orientation, as all values are > 0 . If the texture coefficient data below 350°C is ignored due to the additional hexagonal phases, the untreated samples show a greater tendency to preferred orientation than do the treated samples, which are more random in nature. The texture coefficient of the XRD data from figure 6.10 confirm the general trend of reduced (111) plane and increase in peak intensities of the (220) and (311) planes.

The FWHM for the (111) and (311) peaks are given in table 6.3 and indicate a decrease with increased annealing parameters. Also included in table 6.3 is the Scherrer data determined from the XRD, showing an increase in crystallite size with increased annealing parameters.

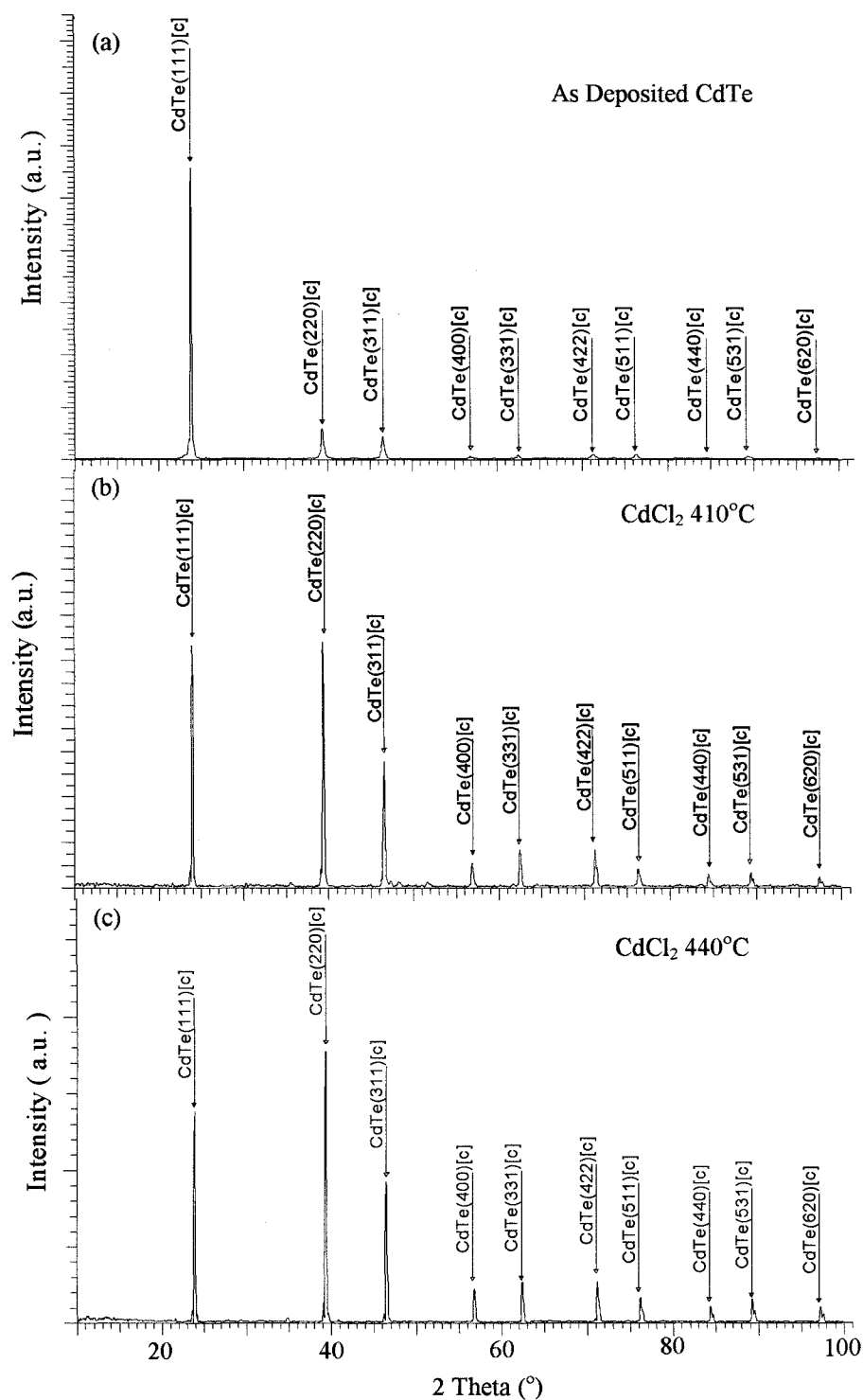


Figure 6.10. XRD Data of As Deposited and CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Varying Annealing Temperatures and Annealing Time of 20 Minutes.

(hkl)	111	220	311	400	331	422	511	440	531	620	N=10
<i>Pdf</i> (%)	1.00	0.60	0.30	0.06	0.10	0.10	0.04	0.02	0.04	0.04	
Tsub (°C)											σ
200	1.441	0.378	8.181	-	-	-	-	-	-	-	2.284
250	1.276	0.802	3.299	0.581	0.349	0.558	1.046	2.091	-	-	0.860
300	1.335	0.952	1.571	0.664	0.664	0.664	0.996	1.328	1.162	0.664	0.320
350	3.614	0.640	0.960	0.727	0.611	0.611	1.527	-	1.309	-	0.878
400	1.698	0.830	0.852	0.361	0.520	0.433	0.758	1.299	2.815	0.433	0.726
Temp CdCl₂ (°C)											σ
410	0.600	1.015	1.049	1.011	0.944	0.944	1.180	1.685	0.899	0.674	0.281
440	0.419	0.897	0.936	1.140	0.828	0.828	1.260	1.170	1.170	0.810	0.327

Table 6.2. Texture Coefficient of Sphalerite Phases Determined from XRD Data for As-Deposited and CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Varying Annealing Temperatures with Annealing Time of 20 Minutes.

Layer	FWHM (111) (2 Theta °)	FWHM (311) (2 Theta °)	Crystallite Size (111) (nm)	Crystallite Size (311) (nm)
As Dep. CdTe (T _{sub} 350°C)	0.222 ± 0.004	0.600 ± 0.012	41.0 ± 1.2	20.0 ± 0.6
CdCl ₂ for 20 mins at 410°C	0.189 ± 0.004	0.341 ± 0.007	48.0 ± 1.4	35.0 ± 1.1
CdCl ₂ for 20 mins at 440°C	0.152 ± 0.003	0.304 ± 0.006	60.0 ± 1.8	40.0 ± 1.2

Table 6.3. FWHM and Crystallite Size Determined from XRD Data of As Deposited and CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Varying Annealing Temperatures with Annealing Time of 20 Minutes.

6.3.2. Optical Properties of CdCl₂ Treated CdTe

The optical properties of the treated coatings were measured to find the energy bandgap and absorptive properties of the CdTe layers. Transmission measurements of the treated samples were obtained with thinner layers, grown using shorter deposition times (layers $\sim 2\mu\text{m}$ thick). The transmittance versus wavelength for a thinner layer, subjected to the same post deposition CdCl₂ treatment, is shown in figure 6.11. These coatings had similar structural properties to that shown in figures 6.10b and 6.10c and the steep absorption edge would indicate that the layers have good crystallinity. The energy bandgap of the treated layer was determined using $(\alpha h\nu)^2$ versus $h\nu$ (using the method described in chapter 5) and was found to be $1.50\pm 0.02\text{eV}$, figure 6.12.

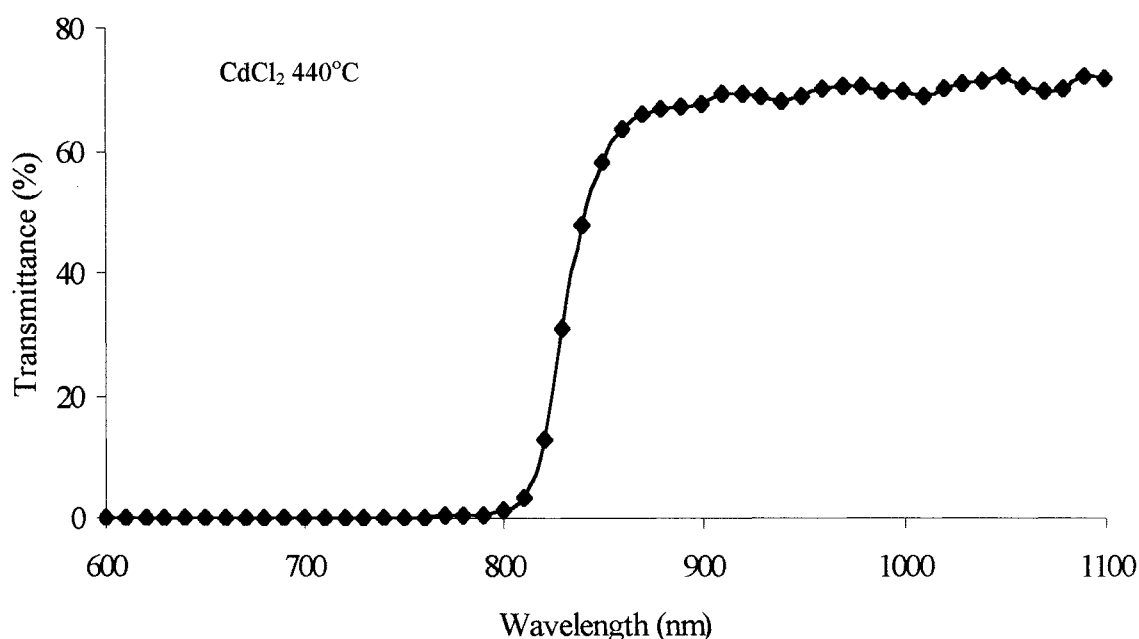


Figure 6.11. Transmittance as a Function of Wavelength for CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Annealing Temperature of 440°C and Annealing Time of 20 Minutes.

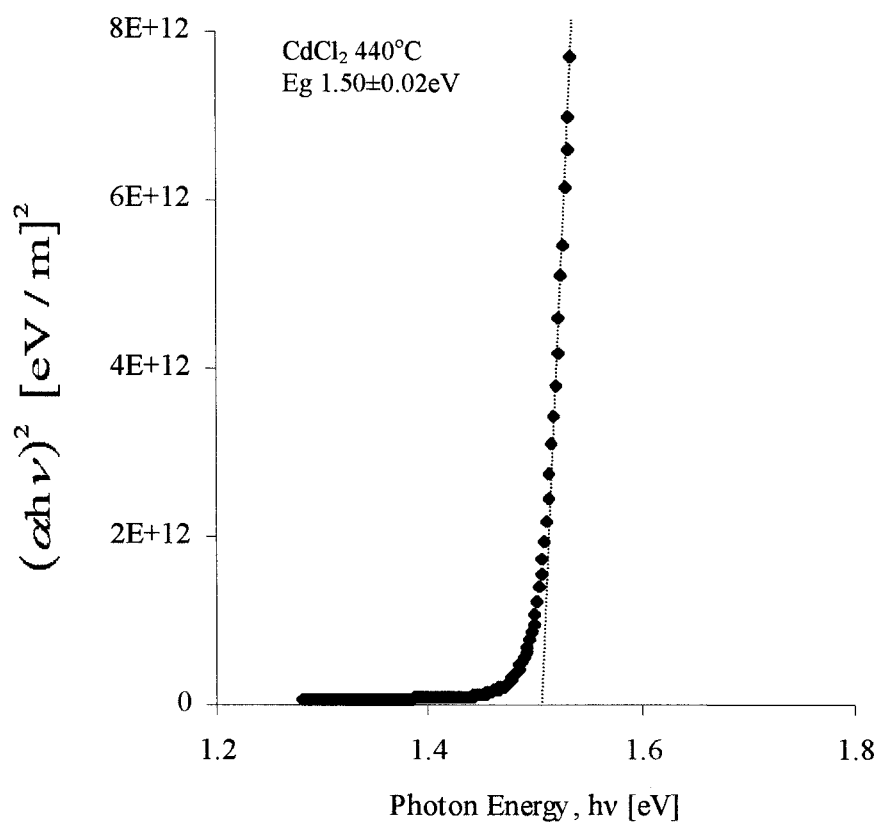


Figure 6.12. $(\alpha h\nu)^2$ as a Function of Photon Energy ($h\nu$) for CdCl₂ Treated CdTe (Dip in 50% Solution for 1 Minute) with Annealing Temperature of 440°C and Annealing Time of 20 Minutes.

6.4 References

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Chapter Seven

ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe Solar Cells Devices

7.1 Formation of a Solar Cell Device

To construct a superstrate configuration solar cell, (see figure 2.21) a number of fabrication steps are required. The deposition chamber was loaded with the buffer and absorber layer materials, as well as the cleaned SnO₂ coated glass. Deposition of the buffer layer was achieved using the procedure described in Chapter 5. However, to confirm their material properties, the buffer layers were removed from the deposition chamber to be characterised by non-destructive methods (such as X-ray diffraction and optical techniques). After characterisation, the coated SnO₂ was placed back into the chamber and the CdTe absorber layer was deposited, using the procedures of Chapter 6. Before the back contacts were made, the CdTe was subjected to an etch. The purpose of this etch is to make the p-CdTe surface more tellurium-rich and in doing so, produce a p⁺ layer that allows easier contacting [1]. The etchant used was a 0.03% bromine/methanol mixture, with the sample dipped into the solution for approximately 30 seconds. All back contacts used for solar cell devices in this work were made using thermally evaporated Au, using a vacuum deposition plant described in section 4.2.3. The final step was to coat the gold contact with a high conductivity silver paint (Adhesion Silver Dag used in microscopy and electronics industry, supplied by Agar Scientific Limited). This step was introduced to protect the thin Au layer from probe damage during characterisation.

7.2 Optimisation of Absorber Layers

7.2.1 Characteristics of Untreated Cells

In Chapter 2, the theory behind the current-voltage characteristics of a solar cell was introduced. The performance of the cell in question can be ascertained by measuring the open circuit voltage (V_{OC}) and short circuit current density (J_{SC}). From the illuminated data, the fill factor (FF) and cell efficiency (η) can be determined using equations 2.49 and 2.50 respectively. Reported solar cell characteristics are, in most cases, normalised to give a cell area of 1cm² [2]. For this work, the fabricated cells in all cases, had an active area less than 1cm². Cell areas were typically 7 to

21mm² and the short circuit current density was scaled up to give an equivalent value to that of a 1cm² cell. The open circuit voltage is unaffected by cell area and was not altered.

The light J-V measurements can also be used to determine the series and shunt resistances of the cell. To estimate the series resistance (R_s), the slope of the J-V curve above V_{OC} was used.

$$R_s \approx \left(\frac{\Delta J}{\Delta V} \right)^{-1} \quad 7.1$$

where $\Delta V > V_{OC}$

Using a similar technique, the shunt resistance (R_{SH}) can be estimated from the slope of the J-V curve at low reverse bias voltage.

$$R_{SH} \approx \left(\frac{\Delta J}{\Delta V} \right)^{-1} \quad 7.2$$

where $\Delta V < 0$.

As with Chapter 5, the optimisation of the buffer layers for use in solar cells was achieved by first using ZnSe. The dark and light J-V characteristics of the cell, without CdCl₂ treatment, are shown in figure 7.1. The thickness of the ZnSe layer in figure 7.1 is 1µm, whereas the thickness of the CdTe is approximately 5µm, a substrate temperature of 200°C was used for the ZnSe and T_{sub} 350°C for the CdTe. The J-V curve produced is typical for the ZnSe or ZnSSe / CdTe cells fabricated without the post deposition chlorine treatment in this work. The shape of this J-V curve would indicate that series resistance is a problem with untreated cells (see figure 2.14a). The thickness of the ZnSe layer greatly increases the series resistance through the cell and the lack of CdCl₂ treatment would indicate that doping of the CdTe layer could be significant.

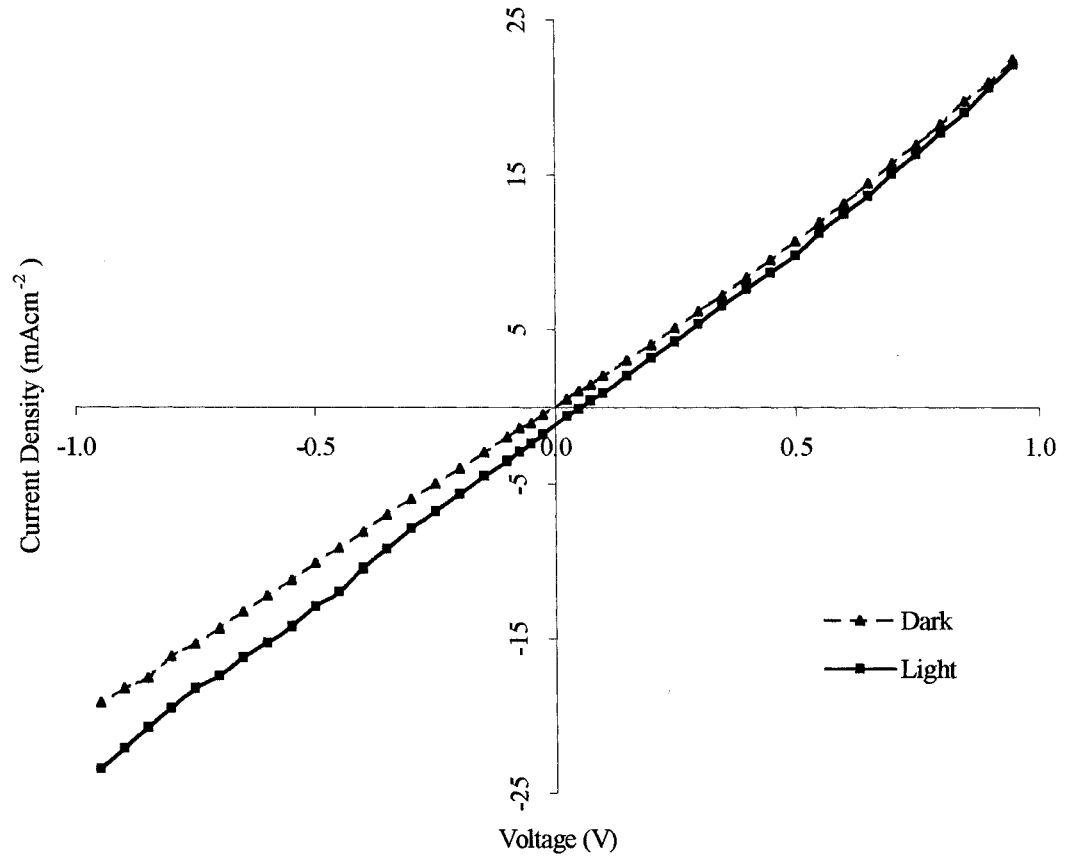


Figure 7.1. J-V Characteristics of an Untreated ZnSe / CdTe Cell.

	V_{oc}	J_{sc}	FF	η	R_s	R_{sh}
	(mV)	(mAcm ⁻²)	(%)	(%)	(Ω)	(Ω)
Light	55	1.1	25	0.02	47	43

Table 7.1. PV Characteristics of an Untreated ZnSe / CdTe Cell.

7.2.2. Characteristics of Treated Cells

Using the CdCl_2 treatment that produced what is believed to be the best CdTe for solar cells (i.e. 440°C for 20 minutes in air) of Chapter 6, an investigation into the optimisation of the absorber layer was carried out. Using the same deposition parameters for the buffer layer of section 7.2.1, (i.e. ZnSe of thickness 1 micron) CdTe was deposited onto glass / SnO_2 / ZnSe, at different substrate temperatures. Each ZnSe / CdTe cell was processed using the same CdCl_2 treatment. A graph of the J-V characteristics and a table showing the cell parameters are shown in figure 7.2 and table 7.2 respectively. The only substrate temperature to show non-linear characteristics is at 350°C . This would appear to confirm the results from chapter 6, suggesting that 350°C is the optimum substrate temperature for CdTe deposited using this technique and treated using this CdCl_2 process. Examining the data of table 7.2, it can be seen that the series resistance, like the shunt resistance, decreases with increased substrate temperature. The open circuit voltage peaks with $T_{\text{sub}} 300^\circ\text{C}$ but is drastically reduced with $T_{\text{sub}} 400^\circ\text{C}$, which coincides with a reduction in shunt resistance. The short circuit current density reaches a maximum of $4.4\text{mA}\cdot\text{cm}^{-2}$ with $T_{\text{sub}} 350^\circ\text{C}$ and produces a fill factor of 28% and an efficiency of 0.4%.

The measurement of quantum efficiency gives an indication of how responsive a cell is to light, at different photon energies. Thin film solar cells will exhibit some form of interdiffusion during high temperature fabrication, which alters the interface between the semiconductor layers. In the example of CdS/CdTe solar cells, the diffusion of tellurium into CdS at short wavelengths can be expected, likewise, with sulphur diffusion into the CdTe layer. However, interdiffusion is more pronounced after the post deposition CdCl_2 treatment [3,4,5]. The diffusion of elements alters the bandgap and therefore absorption coefficient of the CdS and CdTe layers. This in turn alters the spectral response of the cell and can be used as a means to investigate the extent of material interdiffusion [6]. However, it should be noted that interdiffusion is not the only factor affecting the spectral response, recombination, reflection and absorption play key roles in the shape of a cell's responsivity.

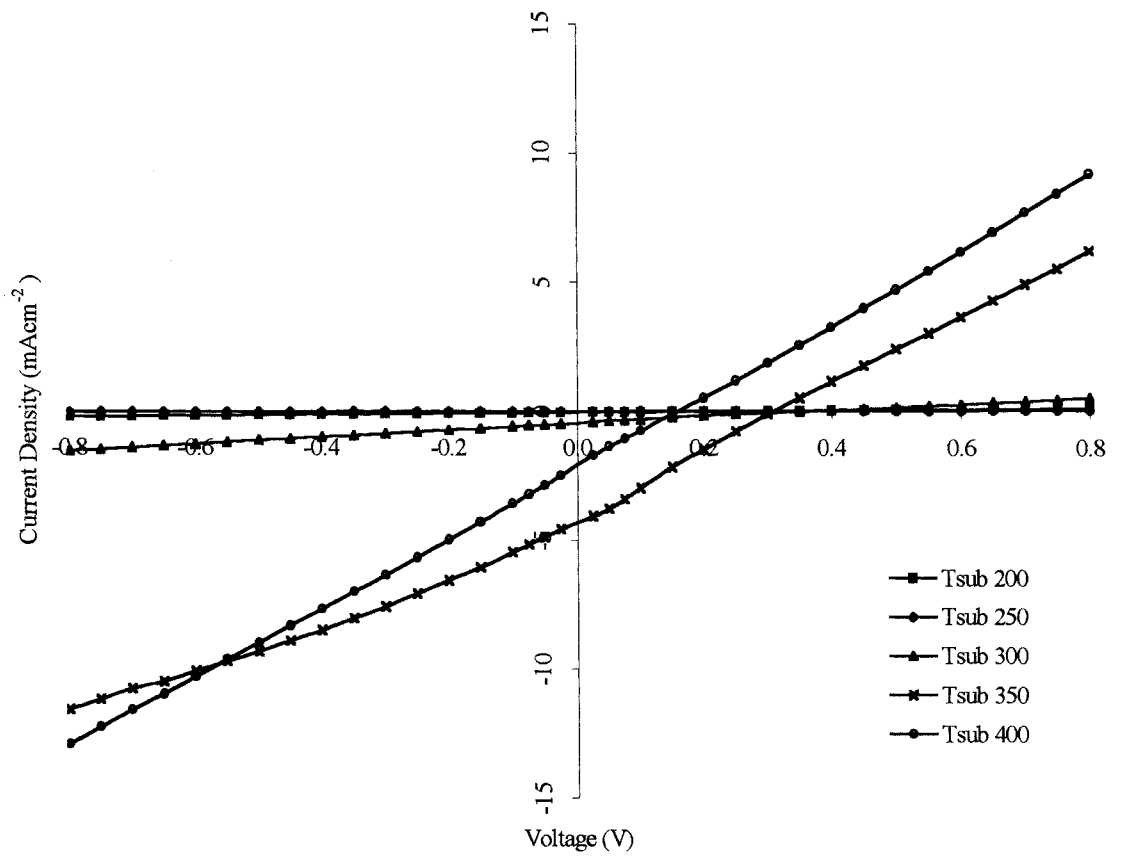


Figure 7.2. J-V Characteristics of ZnSe / CdTe Treated Cells
Grown with Different CdTe Substrate Temperatures.

<i>CdTe</i> T_{SUB}	V_{OC}	J_{SC}	FF	η	R_s	R_{SH}
($^{\circ}C$)	(mV)	(mA.cm $^{-2}$)	(%)	(%)	(Ω)	(Ω)
200	330	0.01	25	0.01	2500	2500
250	350	0.32	25	0.03	1110	910
300	380	0.47	25	0.04	830	670
350	310	4.40	28	0.40	78	116
400	150	2.10	25	0.09	69	74

Table 7.2. PV Characteristics of ZnSe / CdTe Treated Cells
Grown with Different CdTe Substrate Temperatures.

The spectral response of the ZnSe / CdTe cells deposited with different CdTe substrate temperatures is shown in figure 7.3. These data would appear to agree with the results in table 7.2, indicating that the best cell is fabricated using a CdTe substrate temperature of 350°C. It is interesting to note that the spectral response of the cells improve with increased substrate temperature. However, with T_{sub} up to 300°C, there appears to be a lack of response from the wide bandgap material. At short wavelengths, the response edge moves to the wider bandgap position with increased temperature, but at T_{sub} 400°C, the bandedge is once more shortened. This sequence would indicate that the substrate temperature, combined with the CdCl_2 treatment, improves the quality of the ZnSe. If interdiffusion were a factor, then incorporation of tellurium and/or cadmium to form the ternaries ZnSeTe or CdZnSe, and the quaternary CdZnSeTe, would reduce the bandgap (see figure 3.9). This in turn would increase the wavelength of the spectral response absorption edge, which appears to be the case with the T_{sub} 400°C data.

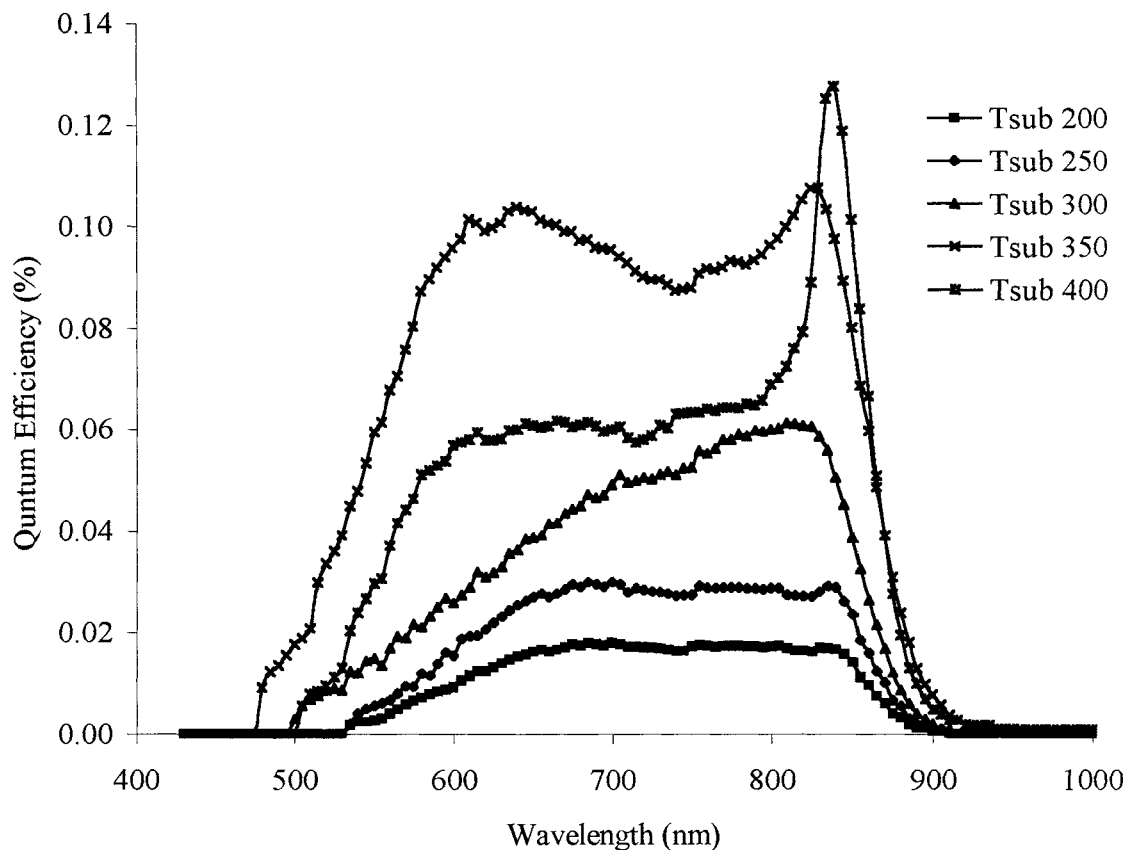


Figure 7.3. Spectral Response of Treated Cells Grown with Different CdTe Substrate Temperatures.

At long wavelengths, the absorption edge shift indicates that the bandgap of the CdTe layer has decreased. Interdiffusion of an element or elements into the CdTe could reduce the bandgap, and in doing so, shift the spectral response long wavelength absorption edge. However, the incorporation of zinc (i.e. CdZnTe) would increase the bandgap of CdTe (see figure 3.9), whereas selenium (i.e. CdSeTe) is a more likely candidate, as this can, depending on the mole fraction, lower the bandgap of CdTe. The large peak in spectral response at longer wavelengths for the 400°C sample would indicate that most of the photocurrent is being generated by the absorber (CdTe) layer. Basol [7] discussed the effect of CdCl₂ treatment on junction position on electrodeposited CdTe. It was stated that a buried junction will produce a larger spectral response in the long wavelength region, whereas a peak in spectral response for short wavelengths is a trait of shallow junctions.

To further investigate the structure of the cells and the possibility of interdiffusion at the junction interface, energy dispersive spectroscopy (EDS) was used. By examining a cross section of the cell, the thickness and interdiffusion of the constituent parts can be examined. The cell was prepared for EDS analysis by cleaving, as other techniques such as mounting and polishing failed to produce good cross-sectional samples. Figure 7.4 shows an SEM image of the cell, with a graph of the atomic distribution superimposed. The cell in figure 7.4 is a ZnSe / CdTe device without CdCl₂ treatment. The ZnSe layer was 1 micron, whereas the CdTe layer was 10 microns thick. The interfaces between the layers are clearly marked by the change in image contrast. Figure 7.5 shows an SEM image and EDS distribution of a cell after CdCl₂ treatment. Interdiffusion at the interface can be seen, as the sharp decline of the Cd and Te in figure 7.4 is not present in this image. This can also be seen by a change in contrast of the SEM image at the interface. The ZnSe distribution has also increased from 1 to approximately 1.5 microns. The change in thickness of the CdTe layer is due to the bromine methanol etch which was applied to this cell prior to contact formation (contacts not shown).

A limitation of this technique is the spacial resolution of the electron beam. Figure 7.6 shows a Monte Carlo simulation of a typical CdS / CdTe solar cell [8]. It can be seen that the resultant X-rays could be from an imaginary cube with sides of approximately 1 micron. Bearing this in mind and examining both the SEM and EDS data together, the atomic distribution clearly matches the perceived cell structure.

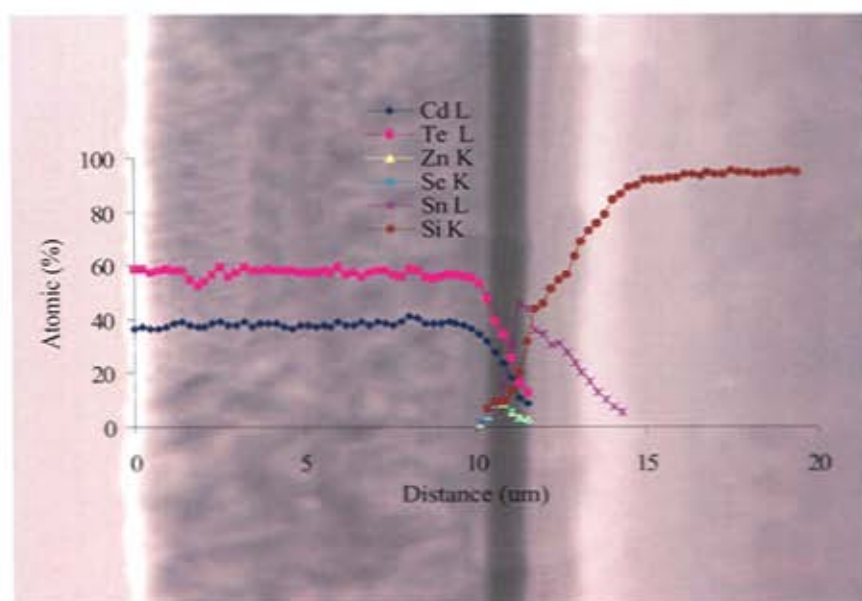


Figure 7.4. Combined SEM Image and EDS Data for an Untreated ZnSe / CdTe Solar Cell, Fabricated with ZnSe T_{sub} 200°C and CdTe T_{sub} 350 °C.

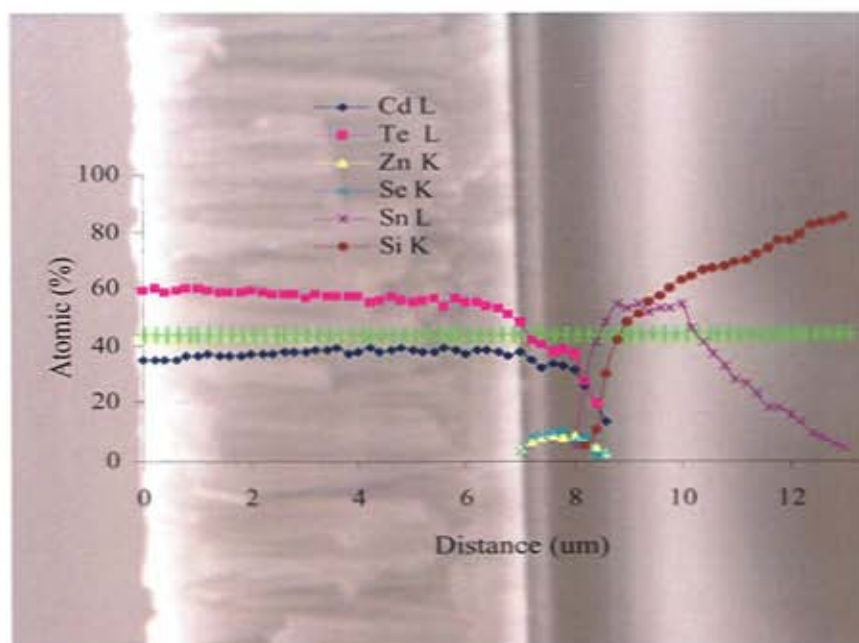


Figure 7.5. Combined SEM Image and EDS Data for a CdCl₂ Treated ZnSe / CdTe Solar Cell, Fabricated with ZnSe T_{sub} 200°C and CdTe T_{sub} 350 °C.

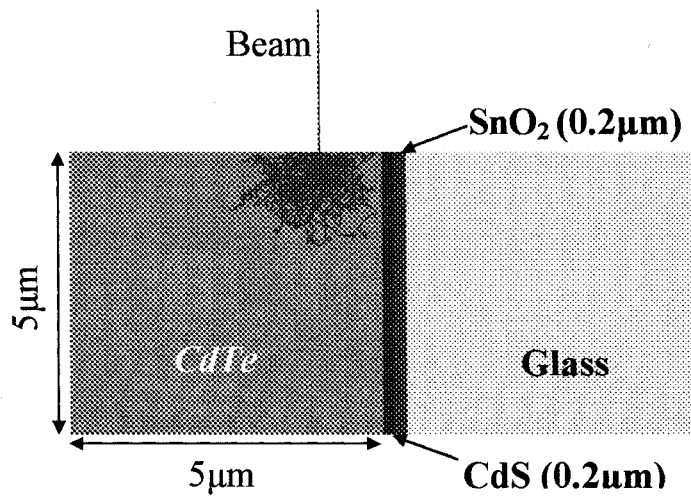


Figure 7.6. Monte Carlo Simulation of a Typical CdS / CdTe Solar Cell.

7.3 Optimisation of Buffer Layers

An attempt to optimise the ZnS_{Se} buffer layers for use in CdTe based solar cells was reported in Chapter 5. However, how successful this process is cannot be determined until the buffer layers, and the absorber layers, are tested in working cells. Therefore to fully optimise the buffer layers, ZnSe deposited with different thicknesses, was again used. After taking into consideration the results of section 7.2, CdTe was deposited at a substrate temperature of 350°C. The post deposition process consisted of (i) a CdCl₂ treatment at 440°C for 20 minutes in air (ii) an etch in 0.03% bromine/methanol for 30 seconds (iii) the addition of thermally evaporated gold contacts (iv) the addition of Silver Dag. The SEM was used to ensure that the deposition time was long enough to produce a CdTe layer (after post deposition treatments) with a thickness of approximately 5 microns. This thickness of CdTe was used in an attempt to minimise the risk of shunting paths through the absorber layer but also not too thick as to increase the series resistance [9,10].

7.3.1 Current Density - Voltage Characteristics

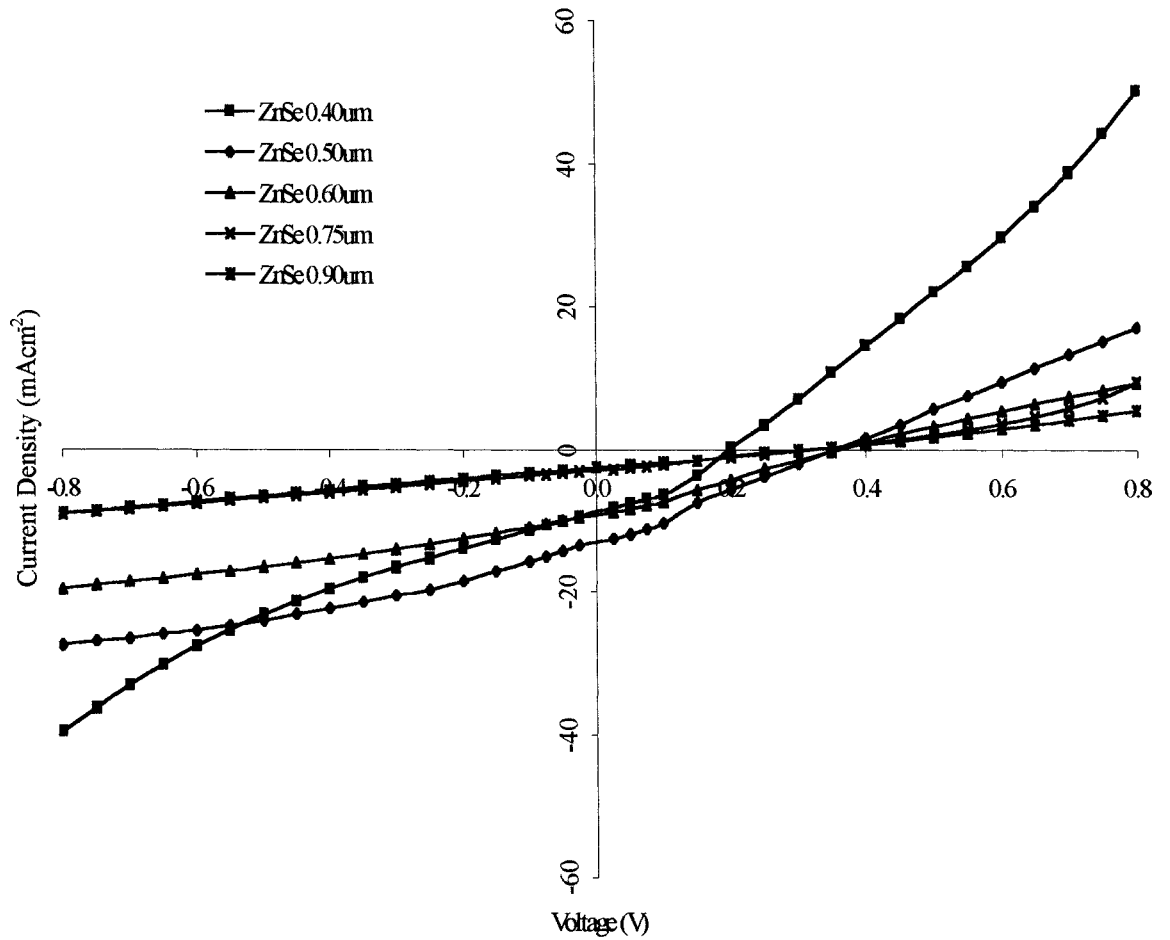


Figure 7.7. J-V Characteristics of ZnSe / CdTe Treated Cells
Fabricated with Different Buffer Layer Thicknesses.

ZnSe Thickness (nominal) (μm)	V_{oc} (mV)	J_{sc} (mAcm^{-2})	FF (%)	η (%)	R_s (Ω)	R_{sh} (Ω)
0.40	200	9.0	36	0.6	12	27
0.50	360	13.0	27	1.2	26	56
0.60	370	9.3	27	0.9	48	76
0.75	330	3.0	26	0.3	72	128
0.90	330	2.6	25	0.2	86	122

Table 7.3. PV Characteristics of ZnSe / CdTe Treated Cells
Fabricated with Different Buffer Layer Thicknesses.

The J-V characteristics of five devices with different buffer layer thicknesses are shown in figure 7.7. The characteristics of the cells are also summarised in table 7.3. The cell with the highest efficiency (1.2%) was fabricated with a buffer layer thickness of 0.5 micron. The open circuit voltage reaches a maximum at a thickness of 0.6 micron, whereas the short circuit current density generally decreases as the buffer layer thickens. The series (R_S) and shunt resistances (R_{SH}) both can be seen to increase with buffer layer thickness. The increase in series resistance, discussed in section 2.2.4 and figure 2.14a, as expected, reduces the short circuit current density. The open circuit voltage however does not follow the shunt resistance to the same degree. The 0.4 micron ZnSe layer has a relatively low V_{OC} which may be due to pinholes, which allow shorting paths, formed during the deposition process [11]. The 0.5 micron and subsequent thicker layers do not appear to suffer too adversely from this phenomenon and reach a plateau at approximately 350mV.

7.3.2 Spectral Response

To further examine the behaviour of the ZnSe buffers in these CdTe based devices, their spectral response was investigated, figure 7.8. The data for the 0.4 and 0.5 micron devices show a similar trend whereupon the CdTe material appears to contribute to the spectral response, but above the ZnSe edge is only partial responsive. At short wavelengths, no absorption roll-off due to the ZnSe bandedge can be found, indicating that the buffer layer is so thin that it does not produce this effect. The two thicker buffer layers of 0.75 and 0.9 microns appear to be too thick. Absorption of photons in the ZnSe layer appears to be reducing not only the short, but also the long wavelength response. The response for the 0.6 micron ZnSe layer shows what could be regarded as the best spectral response for these data. The roll-off of both the ZnSe and CdTe absorption edges can be seen. However, a large amount of recombination, reflection and/or absorption loss, is still evident across the middle section of this cell's response. It should be noted that the discontinuity in the data at approximately 700-750nm is due to the power recorded using a calibrated photodiode.

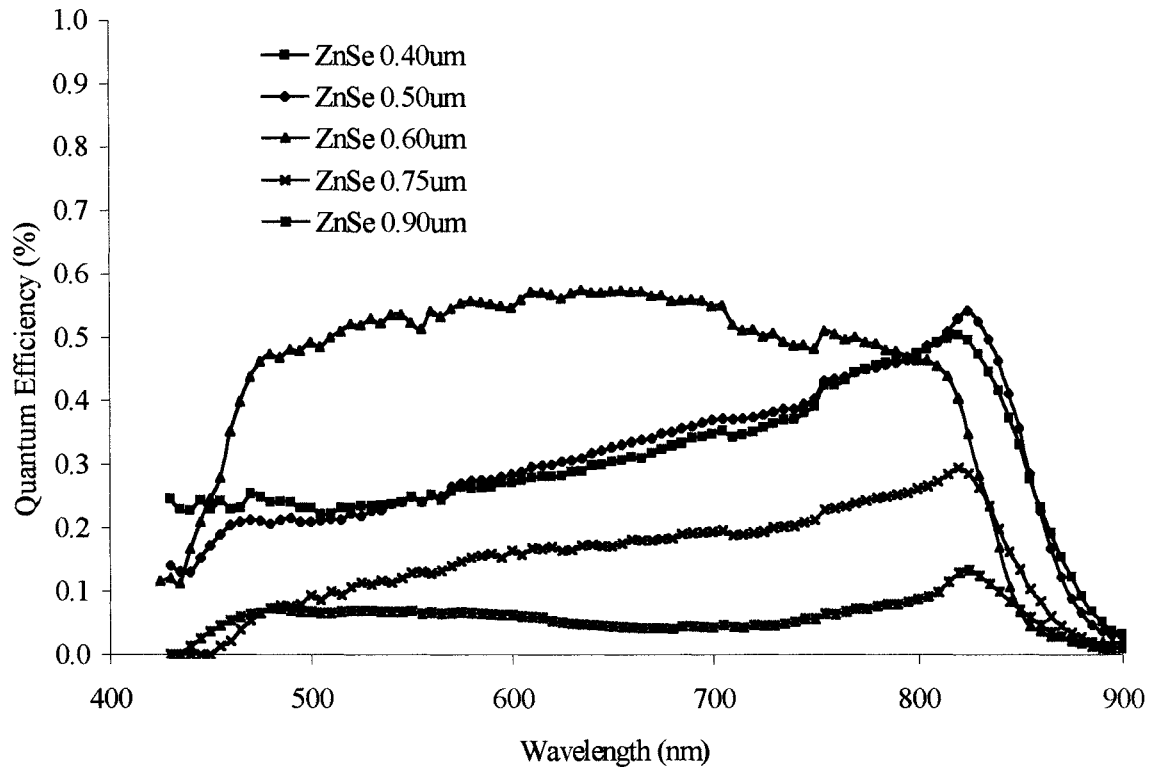


Figure 7.8. Spectral Response of ZnSe / CdTe Treated Cells
Fabricated with Different Buffer Layer Thicknesses.

7.4. Characteristics of CdTe Based Solar Cells

7.4.1. Influence of the Modification of the Buffer / CdTe Interface on Device Performance

The method used to fabricate the devices was again reviewed in order to find the best process for the most efficient solar cell. In section 7.1, the fabrication procedure allowed the deposition of the buffer layers, and section 7.2 of the absorber layers. However, in both cases this involved the removal of the samples from the vacuum chamber and therefore increased the risk of interface contamination. From the outset, the positioning of the boats and samples in the chamber were set up in such a way as to allow deposition of both buffer and absorber layers, without breaking vacuum. Therefore, the buffer layer was deposited, but before deposition of the CdTe layer, the SnO_2 / buffer layers were treated with forming gas. It has been found by other workers [12,13] that by annealing (in most cases CdS) in a hydrogen / nitrogen mixture, ($\sim 10\% \text{H}_2$ / $\sim 90\% \text{N}_2$) a beneficial effect on the material properties is found.

This process appears to clean the layers by removing oxides prior to the absorber deposition.

7.4.2 Fabrication Steps for the Best Solar Cell Devices in this Work

In previous chapters and subsequent sections, the deposition parameters have been revised until the devices made were of a sufficient standard that allows characterisation and investigation of a cell's performance. This culminated in the following fabrication procedure.

- (i) Wash SnO_2 coated glass in degreasing agent (Decon 90) / distilled water, wash for one hour, agitating in an ultrasonic bath.
- (ii) Further wash in distilled water for one hour, again agitating in an ultrasonic bath.
- (iii) Rinse with propan-2-ol (IPA) to reflux the SnO_2 coated glass substrate.
- (iv) Deposit the buffer layer with a substrate-source distance of 11mm, T_{sub} of 200°C and a T_{source} of 600°C , to give a layer thickness of approximately $0.6\mu\text{m}$.
- (v) Anneal in forming gas at 300°C for 15 minutes.
- (vi) Deposit CdTe with a substrate-source distance of 11mm, a T_{sub} of 350°C and a T_{source} of 600°C .
- (vii) Dip in a 50% CdCl_2 (saturated in methanol) / 50% methanol solution for 1 minute.
- (viii) Anneal in air at 440°C for 20 minutes.
- (ix) Etch the CdTe with 0.03% bromine methanol solution for approximately 30 seconds.
- (x) Thermally evaporate gold contacts onto the CdTe.
- (xi) Use Adhesion Silver Dag to improve / protect the gold contacts.

The following sections describe the characteristics of the solar cells showing the “best” photovoltaic performance, all of which were deposited using the fabrication steps described above.

7.4.3. Characteristics of CdS / CdTe Solar Cells

In an attempt to benchmark the ZnSSe / CdTe devices, CdS / CdTe solar cells were produced. The CdS layer was deposited using the optimised procedures previously described, to enable direct comparison. Figure 7.9 illustrates the J-V characteristics of the CdS / CdTe cell showing the best output characteristics in the series. Listed in table 7.4 are the output characteristics of this cell. The open circuit voltage of 530mV is the largest of all the cells reported in this work. V_{OC} is closely related to the shunt resistance and in this cell, R_{SH} is over 400 ohms. The series resistance is also the lowest of all the devices in this work. The series and shunt resistances and the open circuit voltage, combined to give a fill factor of over 46%, again the largest in this work. The efficiency of the cell, assuming AM1.5 conditions, is 2.6%. If, comparing these values to that of table 3.2, then a V_{OC} of over 620mV, J_{SC} greater than 17mAcm^{-2} , fill factors of at least 56% and efficiencies of 10%+ are all larger than reported here.

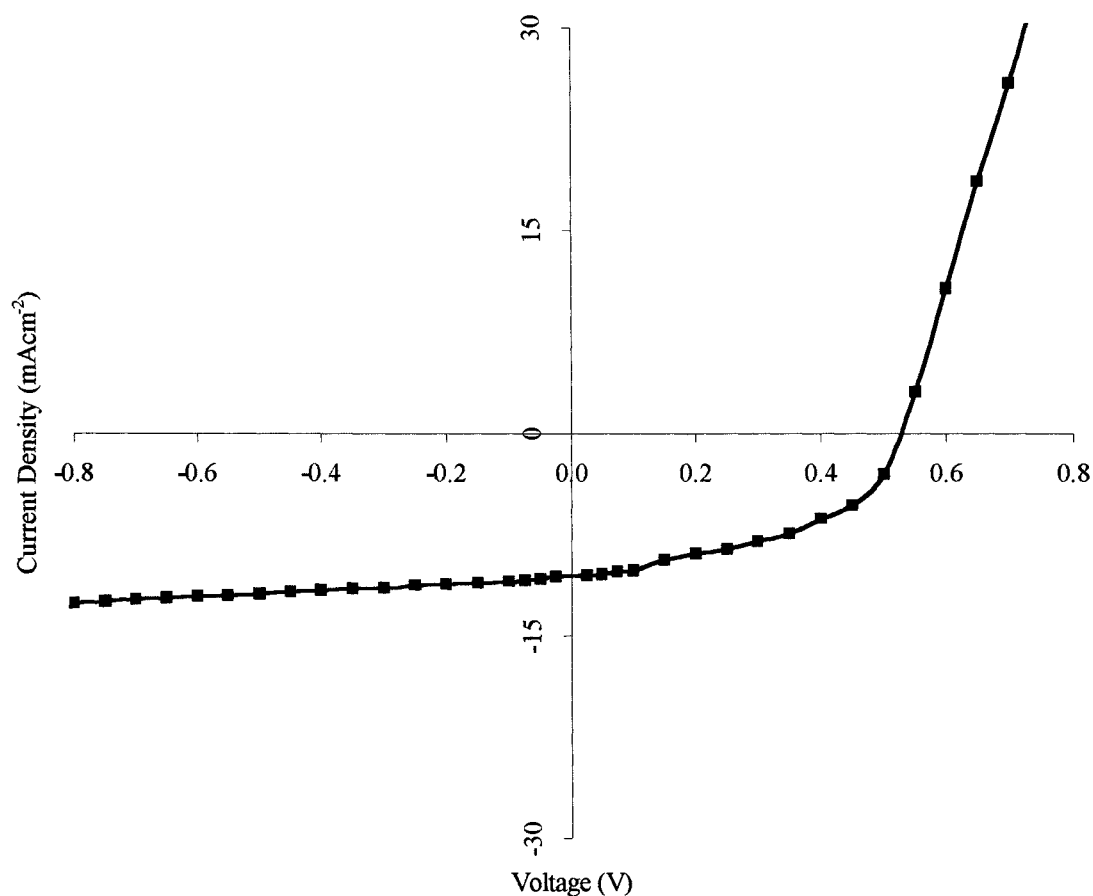


Figure 7.9. J-V Characteristics for CdS / CdTe Cell.

V_{oc}	J_{sc}	FF	η	R_s	R_{sh}	n	J_o	W	Na
(mV)	(mAcm ⁻²)	(%)	(%)	(Ω)	(Ω)		(mAcm ⁻²)	(μ m)	(cm ⁻³)
530	10.5	46.5	2.6	7	416	1.7	5.7×10^{-8}	1.9	8.1×10^{13}

Table 7.4. PV Characteristics for CdS / CdTe Cell.

The spectral response of the above device is illustrated in figure 7.10, the short wavelength response shows a roll-off beginning at approximately 530nm and depreciating from 80 to less than 40%. The responsivity below the CdS bandedge (~510nm) is due to high energy photons passing through the buffer layer, adding to the photocurrent. If the CdS layer were thicker, then these photons would be absorbed before reaching the junction. At longer wavelengths, the photons are expected to be absorbed further in the CdTe layer (i.e. away from the junction) than the high energy photons at shorter wavelengths.

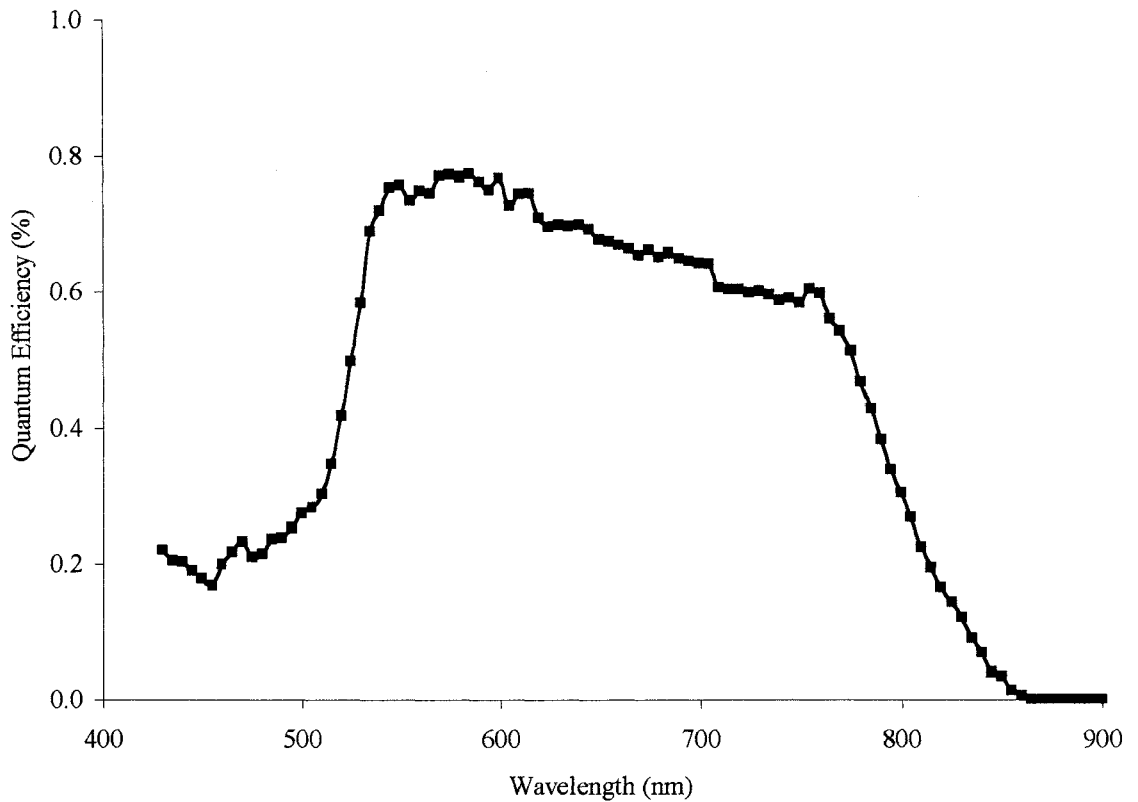


Figure 7.10. Spectral Response for CdS / CdTe Cell.

The minority carrier diffusion length (L_n) affects the conversion efficiency and spectral response, and can be found using [14,15].

$$QE^{-1} = k(L_n + \alpha^{-1}) \quad 7.3.$$

Therefore by plotting QE^{-1} versus α^{-1} and by extrapolation to the horizontal axis, the minority carrier diffusion length can be determined, as illustrated in figure 7.11. The data for the quantum efficiency was taken from the slope of the CdTe edge in figure 7.10, whereas the absorption coefficient data were from [16]. From figure 7.11, L_n is estimated to be $0.18 \pm 0.05 \mu m$ (error in QE data only as absorption coefficient data regarded as constant) which is lower than $0.4 \mu m$ of single crystal CdTe (described as low) [17] and $0.8 \mu m$ for electroless deposition. [18].

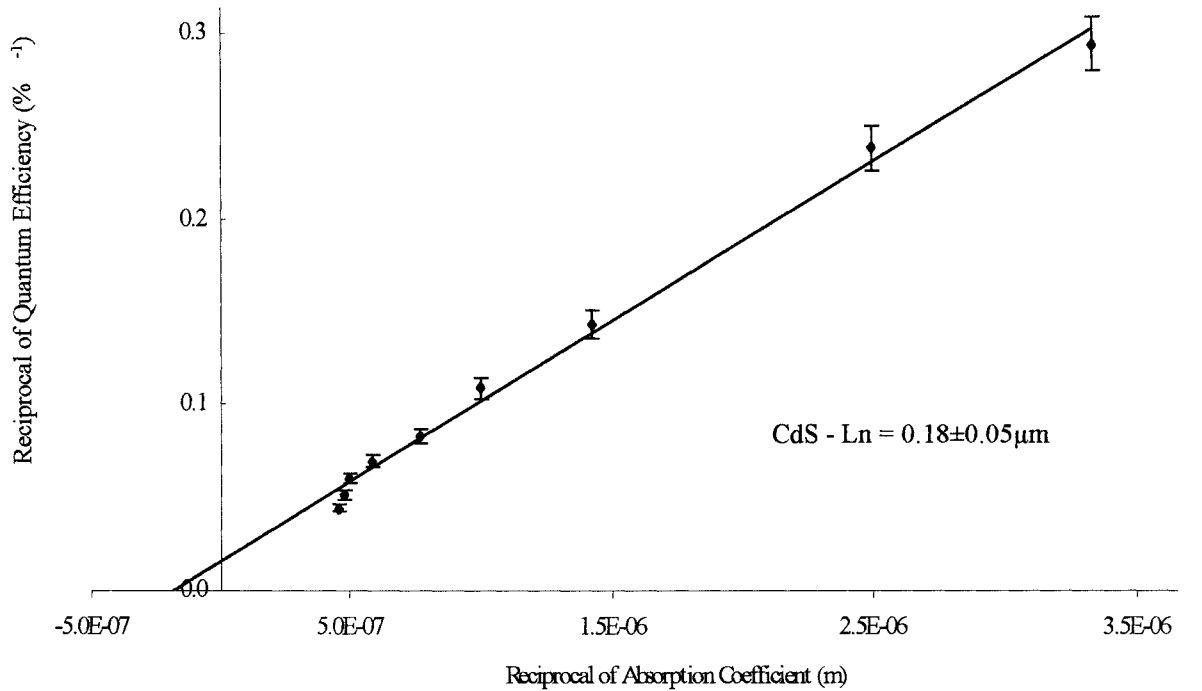


Figure 7.11. Plot of Quantum Efficiency and Absorption Data to Determine the Minority Carrier Diffusion Length (L_n) for CdTe in a CdS / CdTe Solar Cell.

7.4.3.1 Determination of Diode Factor and Reverse Saturation Current

For an ideal solar cell, the diode factor (n) and reverse saturation current (J_o) are not functions of the light illuminating the cell. As shown in Chapter 2, the open circuit voltage can be expressed by

$$V_{oc} = \frac{nkT}{e} \ln \left(\frac{J_{sc}}{J_o} \right) \quad 7.4.$$

Therefore by plotting a graph of $\log_e J_{sc}$ versus V_{oc} , the diode factor, n , can be determined from the gradient and the reverse saturation current, J_o , from the intercept. A set of neutral density filters (300 to 1000 nm) was used to produce the J-V characteristics as a function of intensity. The graph of $\log_e J_{sc}$ versus V_{oc} for the CdS / CdTe cell is shown in figure 7.12.

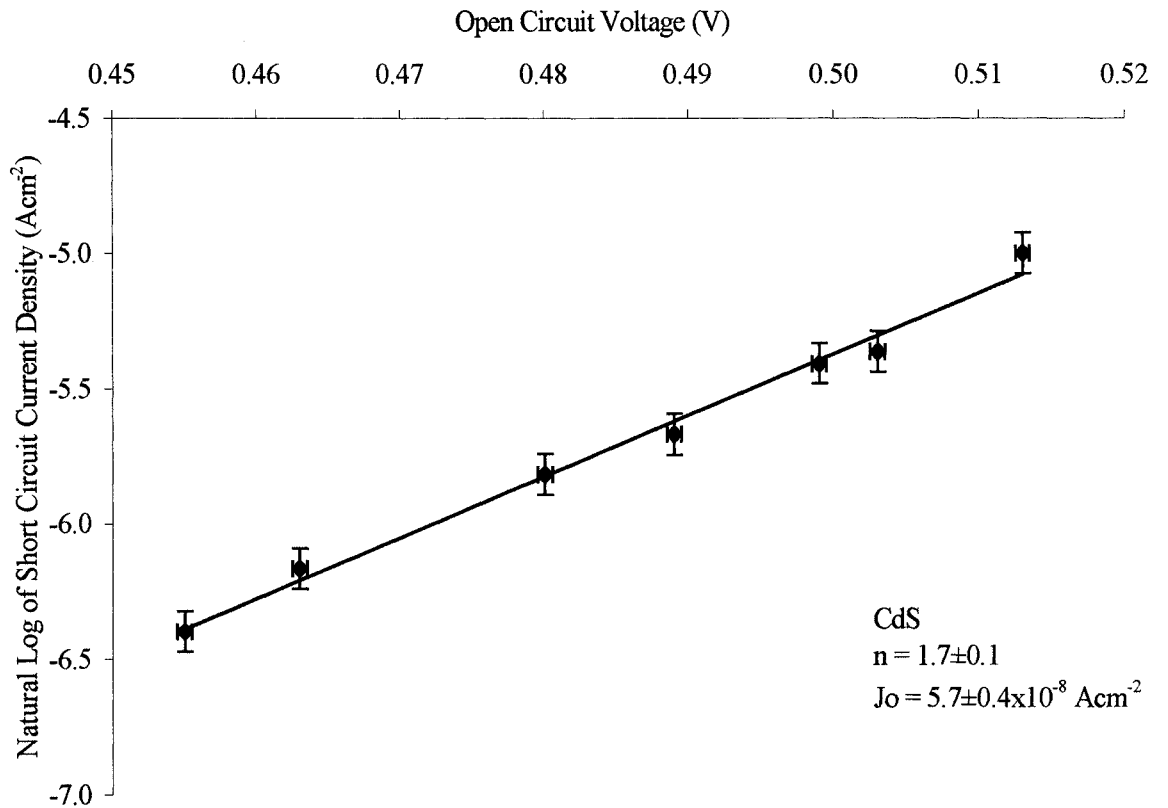


Figure 7.12. Short Circuit Current Density Versus Open Circuit Voltage at Different Intensities for CdS / CdTe Cell

The diode factor and reverse saturation current density for this CdS / CdTe cell were found to be 1.7 ± 0.1 and $5.7 \pm 0.04 \times 10^{-8} \text{ mA cm}^{-2}$ respectively. By examining the results for “best” cells of table 3.2, the diode factor for an n-CdS / p-CdTe device ranges from 1.6 to 2.2 and the reverse saturation current is equivalent to the minimum listed in table 3.2.

7.4.3.2 Capacitance – Voltage Measurements

In chapter 2, the background theory of junction capacitance was introduced. If the assumption is made that the n-region is more heavily doped than the p-region, ($N_D \gg N_A$) then the depletion region should be solely in the CdTe layer. By applying a reverse bias to the junction, the width of the depletion region changes and the single junction approximation equation 2.69, can be rewritten as

$$C_J = \sqrt{\frac{e \epsilon_o \epsilon_r N_A}{2(V_D - V)}} \quad 7.5.$$

where V is the reverse bias. The acceptor concentration of the CdTe (N_A) can be determined from the slope of the C^{-2} versus voltage plots and the depletion width (W) from the parallel plate equation of 2.12, allowing for device area

$$W = \frac{\epsilon_o \epsilon_r A}{C_J} \quad 7.6.$$

All capacitance measurements were taken in the dark, at room temperature, and at a frequency of 100MHz. The graph of C^{-2} versus voltage is shown in figure 7.13. The acceptor concentration was determined from the slope at low bias voltage to be $8.1 \times 10^{13} \text{ cm}^{-3}$. The depletion width, again determined at low bias voltage, was found to be $1.9 \mu\text{m}$. Again comparing with the best cell data of chapter 3, the acceptor concentration is one order of magnitude lower but the depletion width is considerably larger than that reported for the best CdS / CdTe devices (0.54 [19] and 0.19 - $0.29 \mu\text{m}$

[17]) but comparable with CSS deposited CdTe (2.2 to 3.2 μm [20]). The non-linear shape of the C-V curve indicates that the doping may not be uniform through the layer, or interface states could be a problem [21]. However, if the assumption that ($N_D \gg N_A$) is not correct then there is a possibility that the C-V data is from the n-layer (CdS) and may not be uniformly doped. However, Friesen et. al. [22] discussed a dramatic effect the etching process can have on the CdTe doping concentration, investigated with C-V (and impedance) measurements. They concluded that if the etching process is too long, it can induce diffusion through the grain boundaries down to the CdTe / CdS interface and adversely influence the cell's performance.

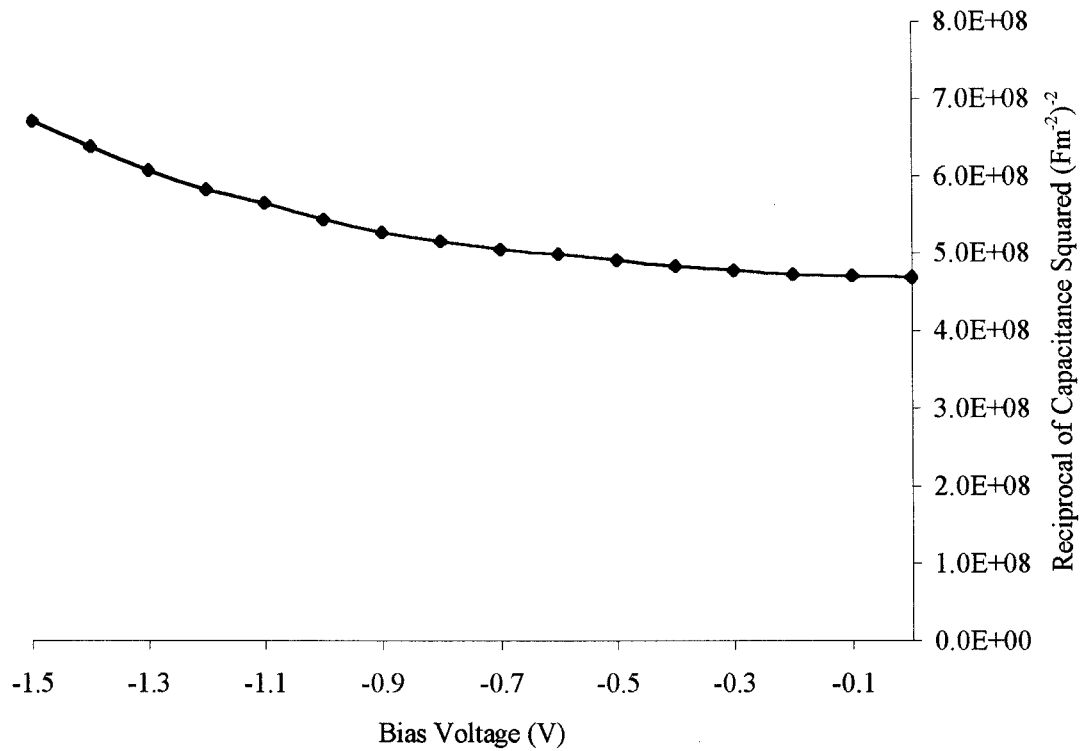


Figure 7.13. Reciprocal of Capacitance Squared Versus Reverse Bias Voltage for CdS / CdTe Cell

7.4.4. Characteristics of ZnSe / CdTe Solar Cell

In the previous section, the “best” CdS / CdTe cell produced during this work was discussed and it is the intention here to use this cell as a means of comparing the ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ buffered cells. The characterisation techniques used in the last section are therefore repeated here. The J-V data of figure 7.14, again shows light induced diode characteristics. Notable differences are the device resistances, see table 7.5. The shunt resistance is reduced to 92Ω (from 416Ω) and this is possibly why the open circuit voltage is smaller. In contrast, the series resistance is larger but the short circuit current density for the ZnSe / CdTe is 17mAcm^{-2} is much larger than the CdS cell. The effect of R_s and R_{SH} is reflected in the lowering of the fill factor to just over 35%. The increase in the short circuit current is the main reason why the efficiency of this cell (2.8%) is larger than that of the CdS cell (2.6%).

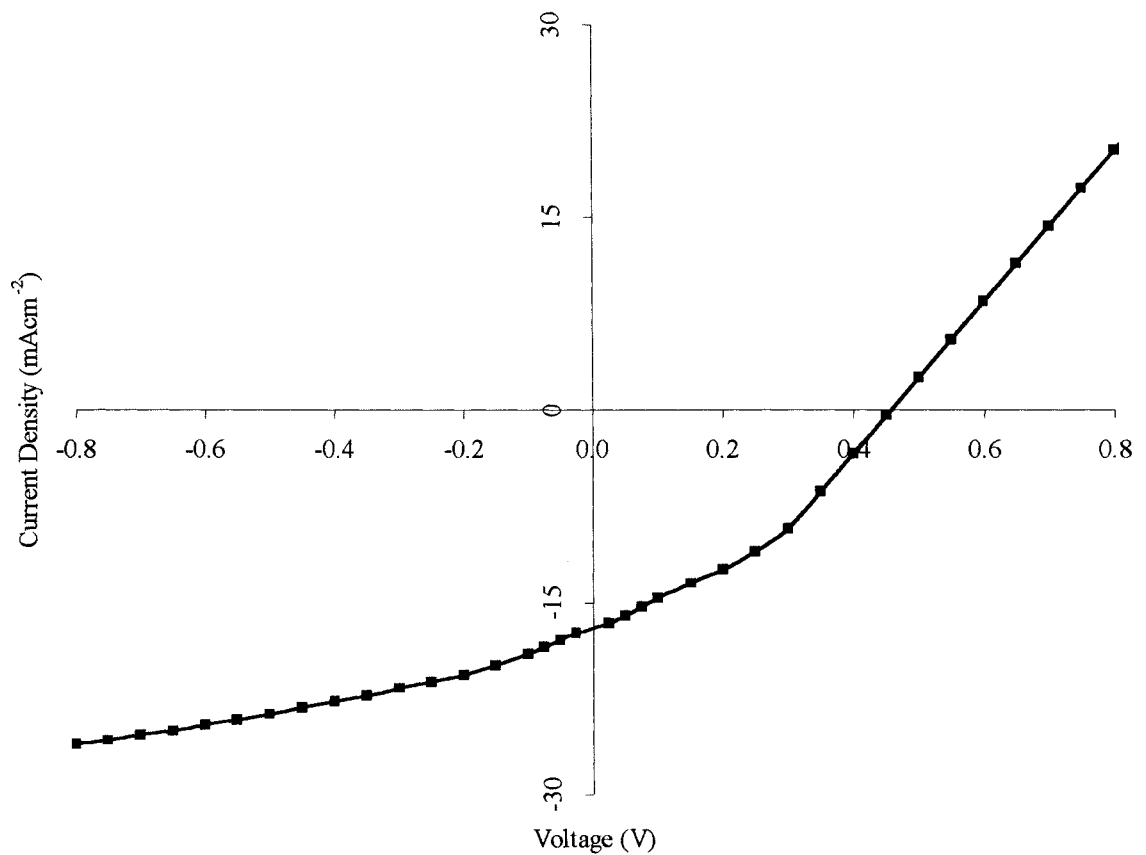


Figure 7.14. J-V Characteristics for ZnSe / CdTe Cell.

V_{oc}	J_{sc}	FF	η	R_s	R_{sh}	n	J_0	W	Na
(mV)	(mAcm ⁻²)	(%)	(%)	(Ω)	(Ω)		(mAcm ⁻²)	(μ m)	(cm ⁻³)
460	17.0	35.6	2.8	17	92	1.6	1.7×10^{-7}	2.4	2.8×10^{13}

Table 7.5 PV Characteristics for ZnSe / CdTe Cell.

The spectral response data illustrated in figure 7.15 indicates a shift in the high energy bandedge, which corresponds to the use of ZnSe ($E_g=2.67\text{eV}$) in place of CdS ($E_g=2.42\text{eV}$). Again, but to a lesser extent, high energy photons are passing through the buffer and contributing to the photo-generated current. At long wavelengths, the bandedge of the CdTe appears to have narrowed, thus moving the low energy roll-off to even longer wavelengths. This is most likely due to interdiffusion at the junction interface. Unlike CdS / CdTe heterojunctions with only one possible ternary alloy available, (CdSTe) the interface of the ZnSe / CdTe cell can produce up to 4 ternaries (ZnSeTe, CdZnSe, CdZnTe and CdSeTe) and one quaternary alloy (ZnSeCdTe). By referring back to figure 3.9, the only ternary alloy that could narrow the bandgap of CdTe is $\text{CdSe}_x\text{Te}_{1-x}$ with x in the region of 0.2. However, this would only reduce the bandgap by approximately 0.1eV. To further investigate this, the minority carrier diffusion length was measured (see figure 7.16) and was found to be $0.13 \pm 0.05 \mu\text{m}$, which is smaller than any of the CdS / CdTe cells of section 7.4.3. Such a low L_n would indicate that recombination could be a problem, which can be seen from the reduction in spectral response between the bandedges. Other workers have produced ZnSe / CdTe heterojunctions using CSVT on single crystal [23] and CSS [24]. The single crystal data showed a large contribution from the high energy photons, (ZnSe) but very little from the low energy (CdTe). For CSS deposited layers, the SR results indicated a contribution across the spectral range, similar to the results of figure 7.15, albeit with a higher quantum efficiency.

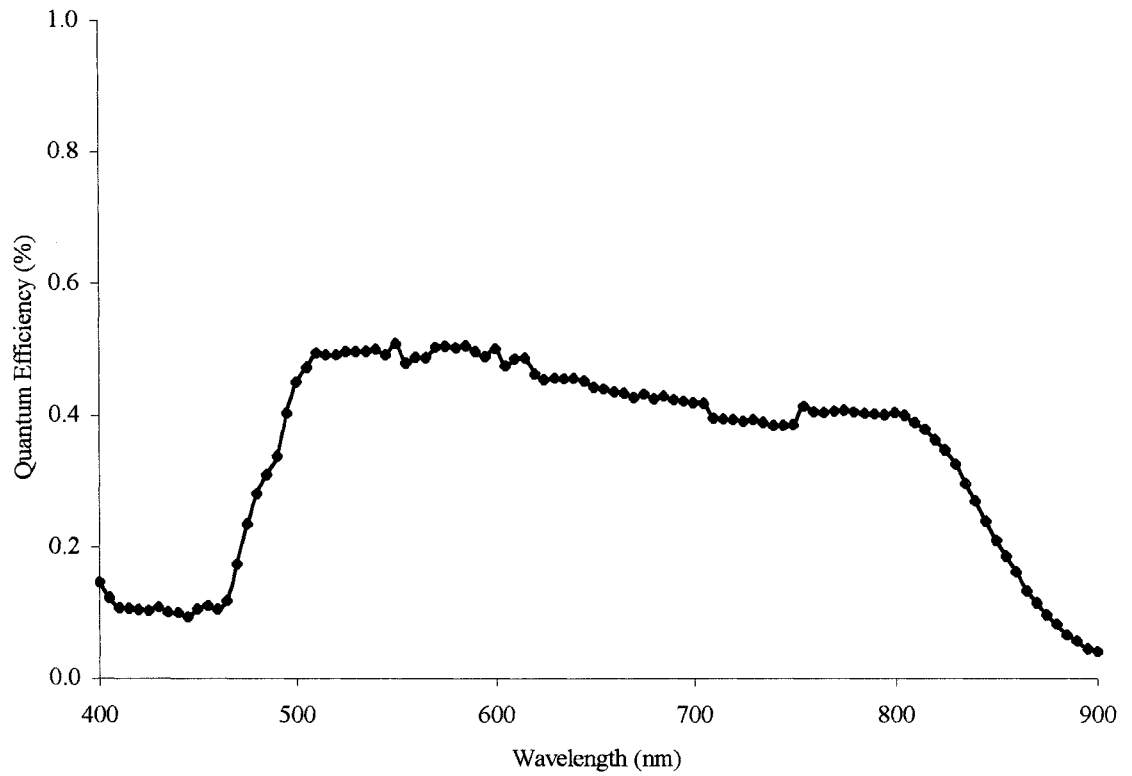


Figure 7.15. Spectral Response for a ZnSe / CdTe Cell.

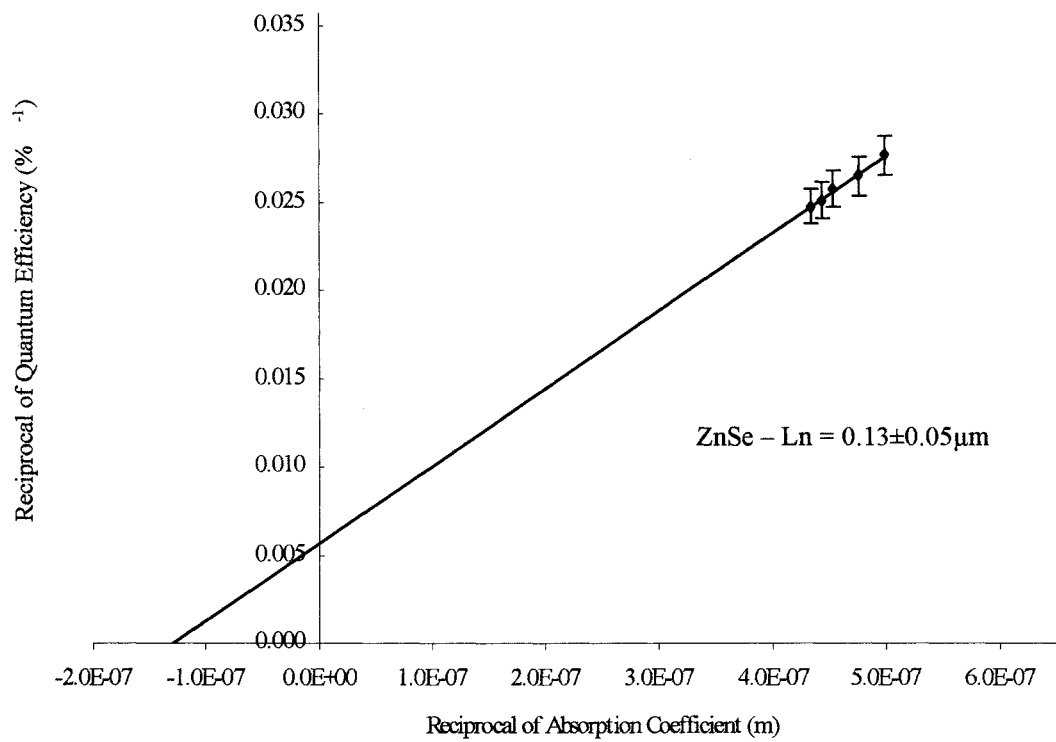


Figure 7.16. Plot of Quantum Efficiency and Absorption Data to Determine the Minority Carrier Diffusion Length (L_n) for CdTe in a ZnSe / CdTe Solar Cell.

Using the same methods as stated in section 7.4.3, n and J_0 were determined from the plot of figure 7.17, whereas W and N_A from the CV data of figure 7.18. The diode factor (1.7 to 1.6), reverse saturation current density (5.7×10^{-8} to $1.7 \times 10^{-7} \text{ Acm}^{-2}$) and acceptor concentration (8.1×10^{13} to $2.8 \times 10^{13} \text{ cm}^{-3}$) all show a slight decrease on the CdS cell data. The depletion width has increased from 1.9 to $2.4 \mu\text{m}$, also the curve for the CV data again indicates a non-linear profile at larger biases.

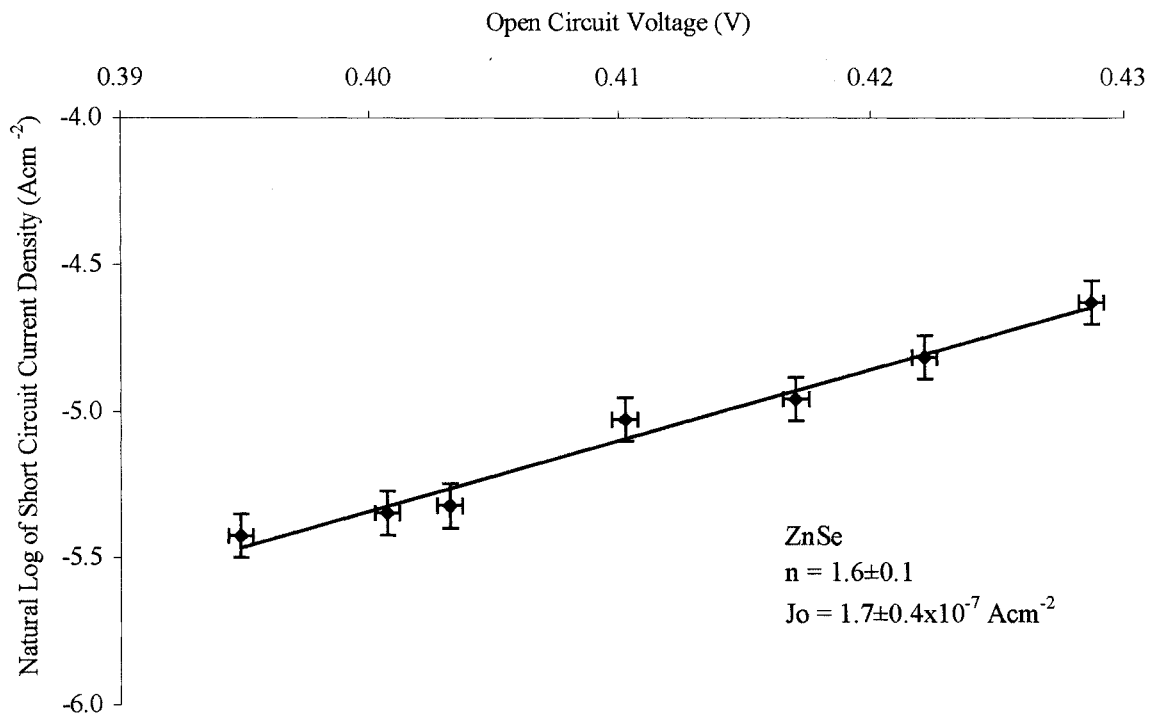


Figure 7.17. Short Circuit Current Density Versus Open Circuit Voltage at Different Intensities for ZnSe / CdTe Cell

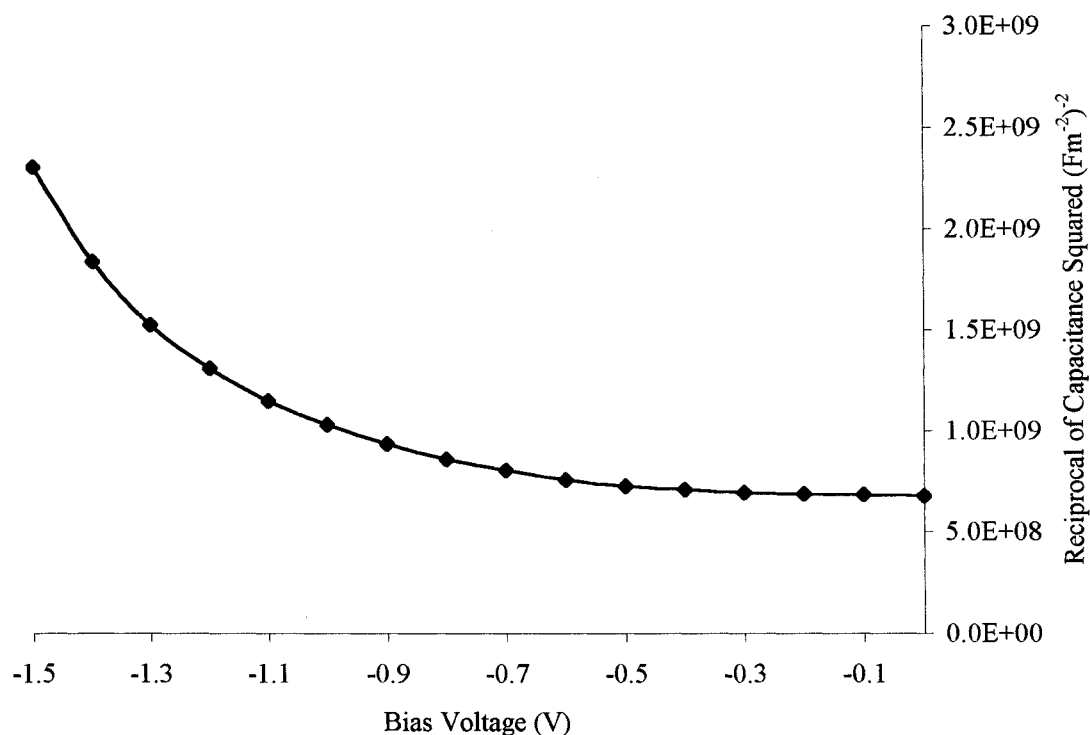


Figure 7.18. Reciprocal of Capacitance Squared Versus Reverse Bias Voltage for ZnSe / CdTe Cell

7.4.5. Characteristics of ZnS_xSe_{1-x} (and ZnS) / CdTe Solar Cells

The ZnS_xSe_{1-x} / CdTe solar cells have again been fabricated and characterised using the same techniques described in the previous sections. The fraction of sulphur in the buffer layer composition is a nominal value, which is an indication of the alloy mixture using the procedures of chapter 5 and the additional data of chapter 7. This is because the best data for the cells (in terms of PV characteristics) was found with devices fabricated without breaking vacuum and hence, without characterisation of the ZnS_xSe_{1-x} layer, prior to CdTe deposition.

The J-V characteristics for the $\text{ZnS}_x\text{Se}_{1-x}$ (ZnS) / CdTe heterojunctions are shown in figure 7.19. The data in table 7.6 indicates the cells in general have poorer photovoltaic qualities with increased sulphur concentration. The cells have comparable shunt resistance but the increased series resistance appears to be reducing the short circuit current and hence hindering the cell's performance.

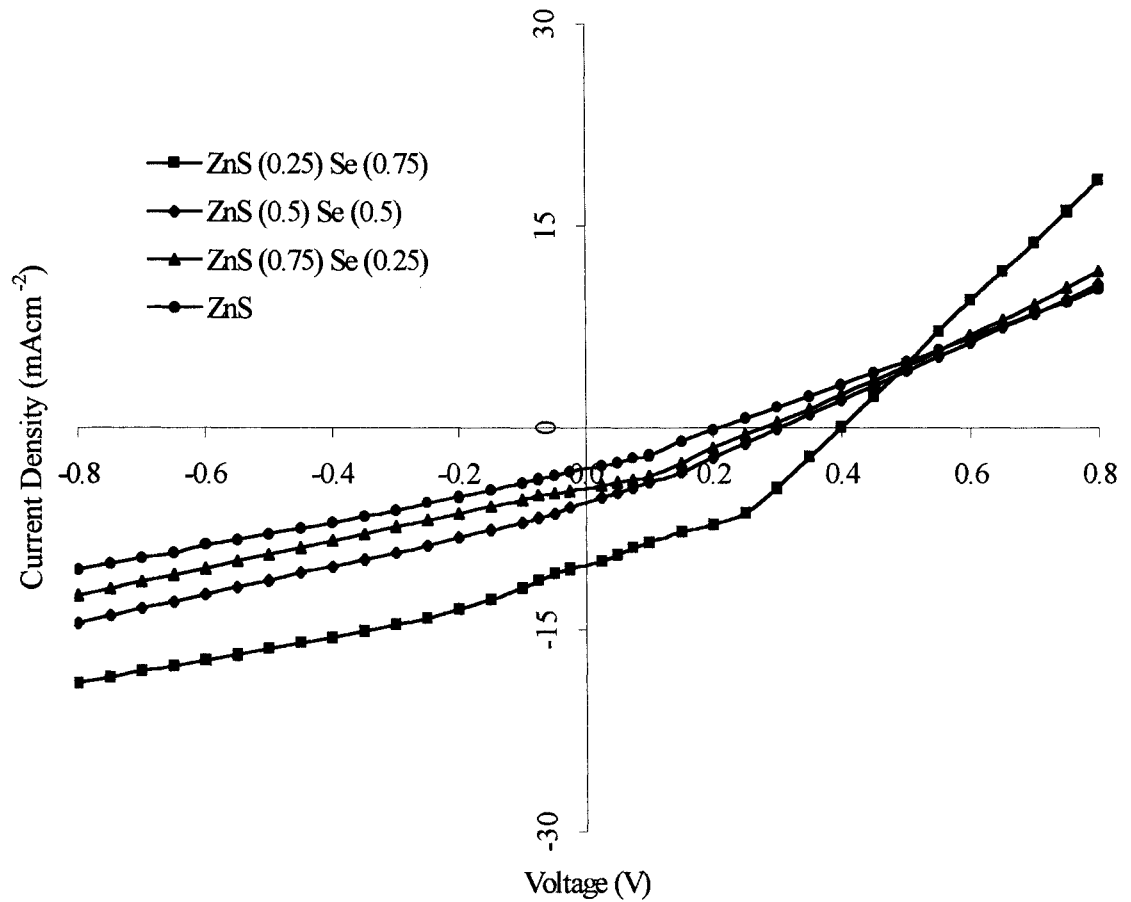


Figure 7.19. J-V Characteristics of $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe Cell

Buffer	V_{oc}	J_{sc}	FF	η	R_s	R_{sh}	n	J_0	W	Na
	(mV)	(mAcm ⁻²)	(%)	(%)	(Ω)	(Ω)		(mAcm ⁻²)	(μ m)	(cm ⁻³)
ZnS _(0.25) Se _(0.75)	400	10.2	38.6	1.6	22	94	2.2	3.5×10 ⁻⁶	3.2	7.5×10 ¹²
ZnS _(0.50) Se _(0.50)	300	5.6	29.5	0.5	47	93	2.3	2.5×10 ⁻⁵	3.9	2.0×10 ¹³
ZnS _(0.75) Se _(0.25)	280	4.5	32.2	0.4	44	99	2.3	1.9×10 ⁻⁵	4.3	5.8×10 ¹²
ZnS	210	3.1	30.2	0.2	57	108	2.5	1.4×10 ⁻⁴	2.7	3.8×10 ¹⁴

Table 7.6. PV Characteristics for ZnS_xSe_{1-x} / CdTe Cell.

The spectral response data for the ZnS_xSe_{1-x} (ZnS) / CdTe devices are shown in figures 20a and 20b. The most notable aspect of these graphs are the high energy cut-off point. By increasing the sulphur content, the energy bandgap of the buffer layer has widened and hence the “spectral window” has increased. However, the lack of high energy photons below the roll-off edge would indicate an increased sulphur content leads to increased recombination. If excessive interdiffusion was taking place at the junction, then any incorporation of Cd or Te would reduce the energy bandgap and reduce the high energy roll-off position, see figure 3.9. At the low energy end, the minority carrier diffusion length (plots shown in figure 7.21) again appears to affect the shape of the response. The data for the minority carrier diffusion length of the ZnS / CdTe cell may not be valid (using this technique was found to be 0.8 μ m), due to the shape of the spectral response of this cell where the QE data was taken from. Also the increased contribution from long wavelengths would indicate that a buried junction has formed [7]. The general shape of the plots shows deterioration in the responsivity with increased sulphur concentration. This culminates in the plot for ZnS / CdTe cell which suggests recombination could be a big problem. Contreras-Puente et. al.[25] reported a ZnS/CdTe cell with the thin film ZnS grown by CBD. Spectral response data showed a large peak at ~700nm, again suggesting a buried junction. However, cells with $J_{sc} = 27\text{mAcm}^{-2}$, $V_{oc} = 320\text{mV}$, $FF = 44\%$, $\eta = 3.8\%$ are all larger than that reported here.

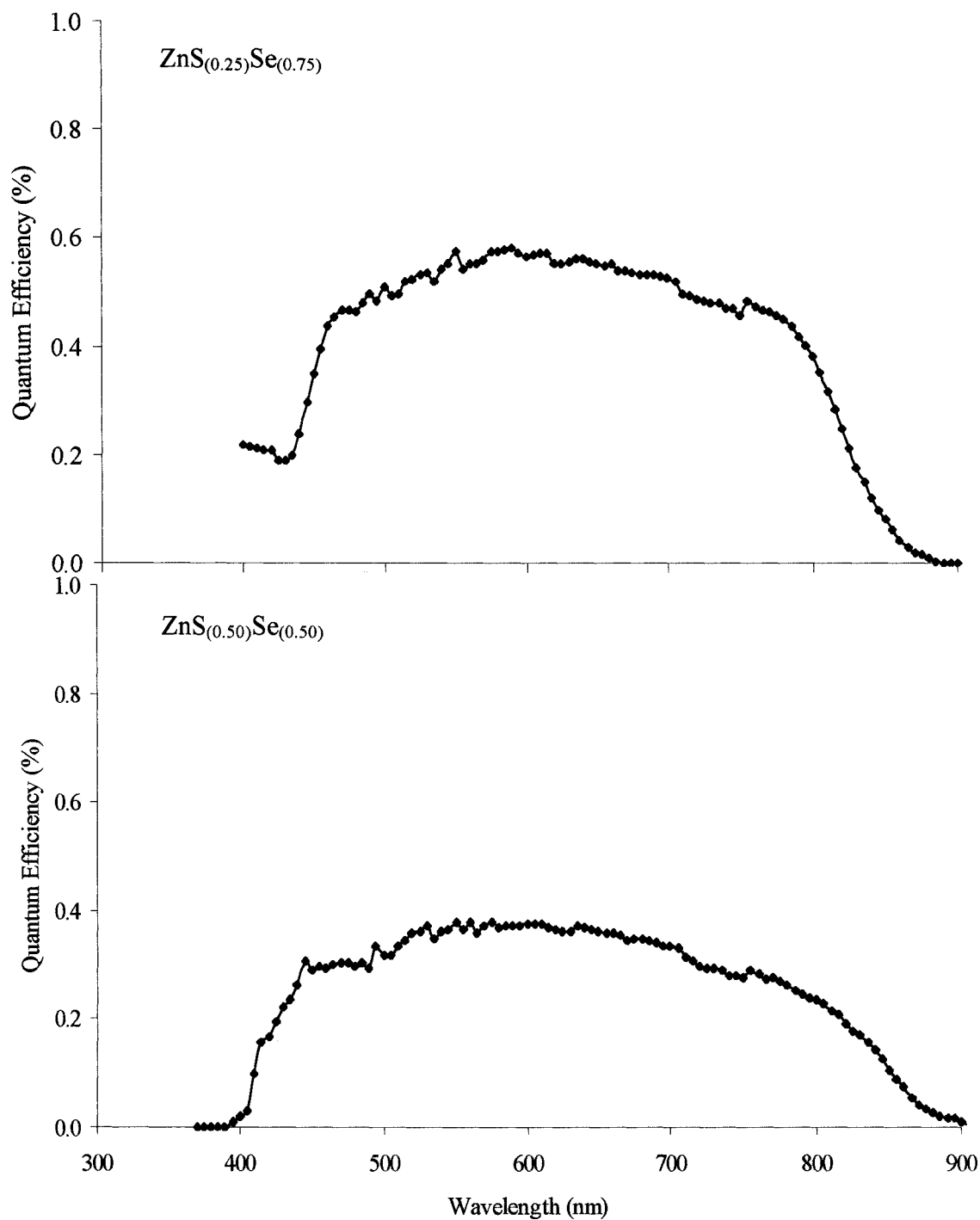


Figure 7.20a. Spectral response for ZnS_xSe_{1-x} / CdTe Solar Cells.

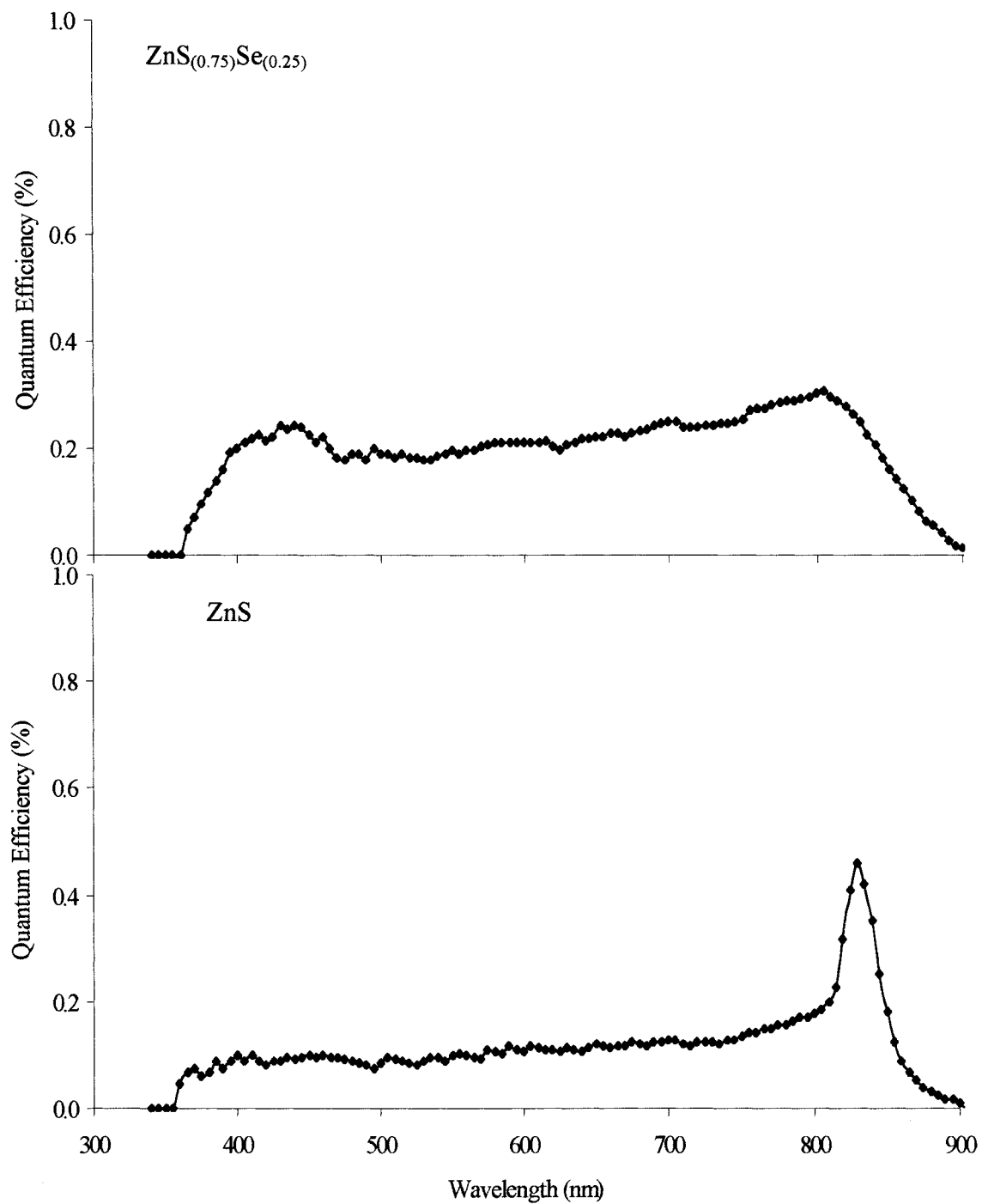


Figure 7.20b. Spectral response for $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe Solar Cells.

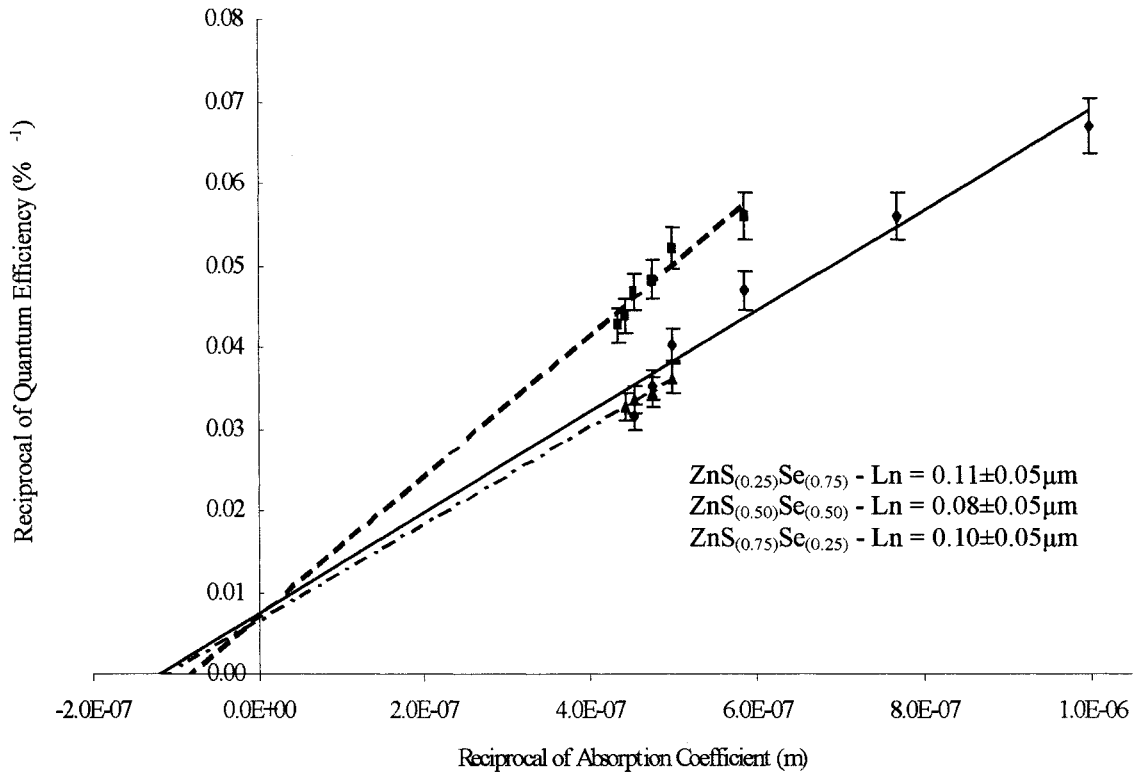


Figure 7.21. Plot of Quantum Efficiency and Absorption Data to Determine the Minority Carrier Diffusion Length (L_n) for CdTe in $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe Solar Cells.

The diode factor and reverse saturation current densities for two cells are shown in figure 7.22 and for the range of buffers listed in table 7.6. These data show that n has generally increased, whereas J_0 has decreased with increasing sulphur content. The data for the depletion width and acceptor concentration were determined from figure 7.23 and are again shown in table 7.6. The depletion width shows a general increase apart from the ZnS cell, whereas there is no apparent trend with the acceptor concentration. These data again shows traits of non-uniform doping or violation of the single sided junction approximation ($N_D \gg N_A$).

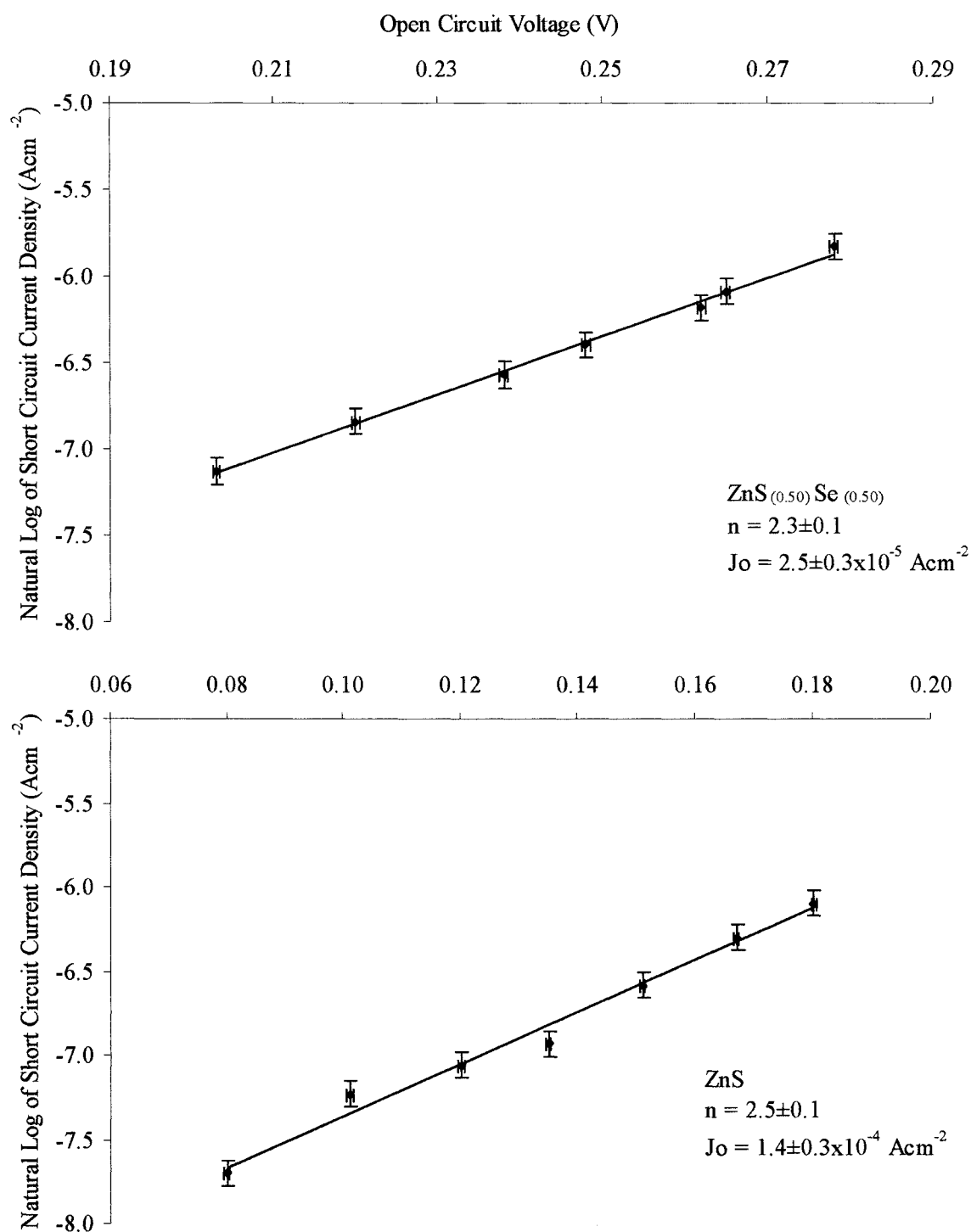


Figure 7.22. Short Circuit Current Density Versus Open Circuit Voltage at Different Intensities for $\text{ZnS}_{(0.50)}\text{Se}_{(0.50)}$ / CdTe and ZnS / CdTe Cells.

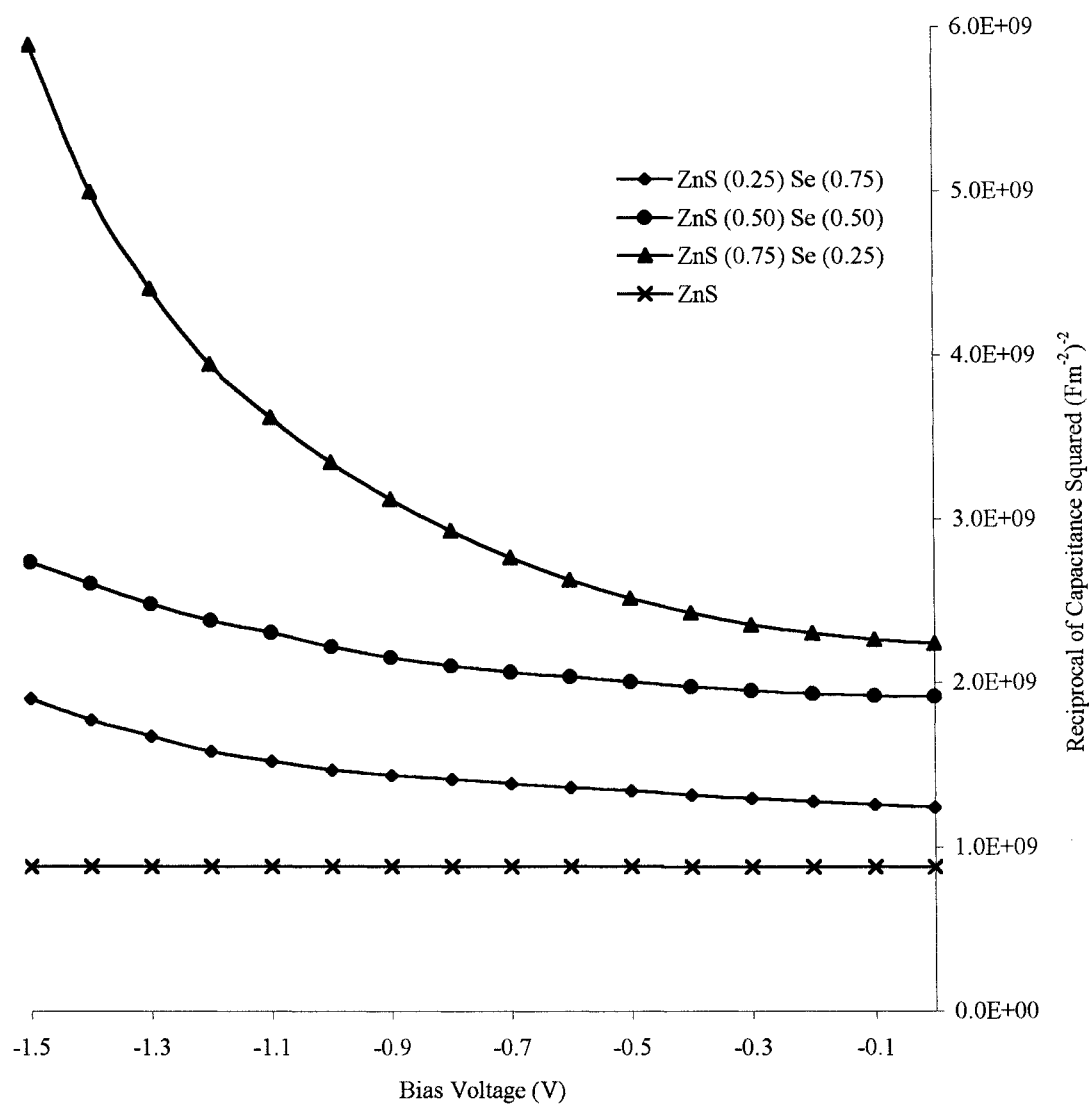


Figure 7.23. Reciprocal of Capacitance Squared Versus Reverse Bias Voltage for $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe Cells

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Chapter Eight

Discussion

8.1 ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers

The morphology of the ZnSe layers has shown to be dependant upon the deposition parameters, not only in terms of source - substrate temperatures, but also source – substrate distance. All ZnSe layers have indicated a general increase in grain size with increasing substrate temperature, which was observed in the SEM micrographs and confirmed from the histogram data. In addition, all ZnSe layers show a change in grain size with source – substrate distance. In terms of smallest grain size, first came the source – substrate distance of 25mm, then 11mm with baffle, and finally the 11mm without baffle. This sequence would therefore indicate that the path length of the vapour stream has increased with the introduction of the baffle, as would be expected, and in doing so has altered the morphology of the films. However, the addition of the baffle is required to produce pinhole free ZnSe (and $\text{ZnS}_x\text{Se}_{1-x}$) layers. The small grain size of these growths, at lower substrate temperatures, would indicate that the deposition process is close to thermal evaporation. However, the larger grains at higher temperatures and higher growth rate would suggest that there are traits of CSS incorporated.

In the case of the $\text{ZnS}_x\text{Se}_{1-x}$ layers, the morphology indicates a general increase in grain size with increasing alloy composition x . This was confirmed from the average grain radius obtained from the histogram data and also AFM micrographs.

The XRD data of the ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers show that all depositions parameters produce a cubic (sphalerite) structure. This is in agreement with the majority of investigations discussed in chapter 3. Also, in all cases, the ZnSe displayed a preferred orientation, with the (111) peak completely dominating. This was followed to some extent by the $\text{ZnS}_x\text{Se}_{1-x}$ layers and was also found by [1] for alloy compositions up to $x = 0.6$.

The X-ray diffraction data was used to determine the alloy composition, assuming that Vegards law applies to this alloy system, as used by other workers [2]. A non-linear relationship between the end binaries was found for the energy bandgap and was fitted to a quadratic equation. The optical bowing parameter was determined to be $0.51 \pm 0.05 \text{ eV}$. This is in agreement with $\text{ZnS}_x\text{Se}_{1-x}$ [3] deposited by vacuum evaporation, and also close to the average bowing value of approximately 0.6 eV , found with other growth methods discussed in chapter 3.

The optical properties of the ZnSe layer produced at a distance of 25mm indicated some problems with the deposits, as transmittance and absorption edges were poor, even though the effects of coating thickness could be neglected. This was not the case for the other ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ growths, where steep absorption edges and good transmittance in the pass region were found. Therefore, it is postulated that the problems with the 25mm coatings are a function of the structure, possibly caused by the stoichiometry leading to either excessive absorption, or reflection of the incident radiation, as this did not affect the bandgap of these layers.

The energy bandgaps for the ZnSe layers, obtained from the optical data, show a variation with substrate temperature. This could be due to impurity levels that have been inadvertently introduced during deposition. However, the data for a substrate temperature of 200°C systematically show the “best” optical properties, with bandgaps near to the accepted value of 2.67eV for ZnSe [4]. This is also confirmed by the smooth curve obtained for the energy bandgap as a function of alloy composition for the $\text{ZnS}_x\text{Se}_{1-x}$ growths, which were also deposited with a source temperature of 200°C.

The structural and optical data indicate excellent mixing of the sulphur and selenium anions producing homogenous alloys. However, the ratios of the powders before deposition does not entirely agree with the material results after growth. This is possibly due to the different vapour pressures of the two end binaries, but the stoichiometry of the layers has to be considered.

When examining the morphology it was found that most layers required a gold coating, as conductive samples are required when using the SEM. This was therefore used as an indicator to resistivity of the coatings and is why no electrical data is presented for the as-deposited ZnSe layers. A similar situation was found for the $\text{ZnS}_x\text{Se}_{1-x}$ layers. To overcome this, thinner layers of $\text{ZnS}_x\text{Se}_{1-x}$ were produced on SnO_2 coated glass substrates to which In contacts were added, to enable the series resistance through the layer to be determined, producing layers with $R_s < 60\Omega.\text{cm}^2$.

8.2 CdTe Layers

By restricting the plant set up to that which produced successful $\text{ZnS}_x\text{Se}_{1-x}$ layers, initial deposition of the CdTe films proved to be problematic. As with the $\text{ZnS}_x\text{Se}_{1-x}$ source temperature of 500°C , surface integrity was a problem with early depositions of CdTe. However, by increasing the source temperature to 600°C , and adding a baffle, the CdTe layers were uniform and pinhole free. The grain sizes of the as-deposited layers have shown a general increase in size with substrate temperature determined from the XRD data (ignoring hexagonal structures). The morphology of the as-deposited CdTe layers show small structures, which have more in common with thermal evaporation than close-spaced sublimation. Thermal evaporation coatings generally have small grains, prone to grain growth by the CdCl_2 treatment, whereas CSS structures do not tend to show growth as the as-deposited grains are already large in comparison. The CdCl_2 post deposition treatment in this work did produce large grain growths, confirming that the deposition technique used for the CdTe is closer to vacuum evaporation than CSS. Moutinho et. Al. [5] discussed the properties of CdTe films grown by physical vapour deposition (PVD) and CSS. Their PVD data show similar properties to the CdTe and CdCl_2 treated CdTe produced in this work. In addition, growth rates of $0.02\mu\text{m}\cdot\text{min}^{-1}$ ($T_{\text{sub}} 250^\circ\text{C}$ at 10^{-5} Torr) and $6\mu\text{m}\cdot\text{min}^{-1}$ ($T_{\text{sub}} 590^\circ\text{C}$ in 0.1 Torr of N_2) were found for the PVD and CSS respectively. The growth rate of $\sim 1.62 \pm 0.04\mu\text{m}\cdot\text{min}^{-1}$ determined in this work would therefore indicate a CSTE deposition process between thermal evaporation and CSS.

The structural aspects of the lower substrate temperature ($< 300^\circ\text{C}$) show signs of mixed phases, however at higher temperatures, only the cubic phase prevails. It is postulated that this is caused by randomisation in the form of structural defects, which are removed at elevated temperatures for both as-deposited and CdCl_2 treated samples.

Transmittance data from the as-deposited CdTe could not be obtained as the coatings were opaque above the absorption edge. After the post deposition heat treatment, this was not a problem (with thin layers) and this would suggest that there is instead a problem with film stoichiometry. However, EDS data (shown in chapter 7) of as-deposited and treated cells show the same CdTe structure (Cd 40 to 45at.%, and Te 55 to 60at.%).

The as-deposited CdTe layers were prone to high resistances, indicated by charging effects found when trying to observe the uncoated samples in the SEM. After CdCl₂ treatment, these layers became much more conductive, to the point where hot probe measurements could be undertaken and the negative deflection indicating a p-type conversion of the CdTe.

8.3 ZnSe and ZnS_xSe_{1-x} / CdTe Solar Cells Devices

Initial results with untreated cells (no CdCl₂ treatment) indicated a linear relationship between the current density and voltage. These cells do indicate some PV characteristics as small short circuit current densities and open circuit voltages were produced. However, the lack of CdCl₂ treatment would suggest that the CdTe layer is only lightly p-type doped. A second consideration is the effect the CdCl₂ treatment has on the buffer layers. If the ZnSe is only weakly n-doped then the operation of the cell would again be adversely affected. Finally, the thickness of these layers should be discussed, the ZnSe layers were 1µm whereas the CdTe layers were 5µm thick. In both cases these layers could be considered thicker than actually required. This was implemented to ensure that no shorting paths (that reduce R_{SH}) and complete optical absorption was achieved, however this may be due to the detriment of the series resistance.

Introducing the optimised CdCl₂ treatment (of chapter 6) the PV properties of the cells were investigated (with identical fabrication parameters). Using the same deposition parameters as the untreated cell of section 7.2.1 (T_{sub} ZnSe 200°C and T_{sub} CdTe 350°C) the PV properties were improved, thus indicating that the CdCl₂ treatment is a critical processing step with CdTe based cells. Other workers (see section 3.5) have shown that the CdCl₂ treatment dopes and improves the crystallinity of the CdTe layer. In addition, improvements to the buffer layers (most cases CdS) have also been reported (again section 3.5). Unfortunately these ZnSe layers still suffer from large series resistances which are affecting the short circuit current densities. This is most likely due to series resistance of the bulk regions but may also be from the n-p interface or back contact.

The spectral response of the cells with buffer layers 1µm thick indicate that recombination is a problem as low quantum efficiency is found. The spectral response

data was also used to examine the interdiffusion at the interface. These data indicate that interdiffusion is more pronounced with higher temperature processing as would be expected.

Using what was considered to be the optimised absorber layer fabrication parameters (deposition and post deposition), an investigation was carried out into optimising the buffer layers. As reported in Chapter 5, the series resistance of SnO_2 / $\text{ZnS}_x\text{Se}_{1-x}$ / In was reduced by depositing thinner buffer layers. By using thinner layers than that of section 7.2 it was found that the PV characteristics could be improved. This culminated in the best combined J-V and spectral response data, indicating an optimum buffer layer thickness of $0.6\mu\text{m}$.

The fabrication procedure was further reviewed, culminating in a sequence of eleven steps to produce a solar cell for testing purposes. In an attempt to bench mark the zinc buffered devices, CdS / CdTe solar cells were produced. The characteristics of the CdS cells produced the best performance, in terms of PV and spectral response, of all the cells in this work. However, it should be noted that no attempt was made to optimise the CdS layers and there is scope for further improvement.

The method used to determine the minority carrier diffusion length for the CdS / CdTe device, found $L_n = 0.18\mu\text{m}$, which is smaller than most values discussed in Chapter 3. However, the technique itself appears to be prone to errors as the slope of the QE data does not necessarily produce enough data points to allow extrapolation to the horizontal axis (e.g. see figure 7.16). A better technique would be to use electron beam induced current, EBIC (not available during these investigations). This method uses the main beam of an electron microscope to scan across a cleaved sample, producing a distribution map of the current as a function of distance. Not only can the minority carrier lengths of the CdTe and buffer layer be resolved from the slopes of the graph, but also the junction position can be determined.

The CdS / CdTe data for the ideality factor and reverse saturation current are comparable to that of the literature with measurements taken from the illuminated properties of the device. To determine the depletion width and acceptor concentration, C-V measurements were undertaken. The assumption was made that the n-region is more heavily doped than the p-region ($N_D \gg N_A$) and in which case the single sided junction approximation can be used (equation 7.5). Measurements taken at low bias voltages indicated depletion widths larger than single crystal devices, but comparable to CSS deposited CdTe and acceptor concentration an order of magnitude lower.

However, the shape of the CV data would indicate there may be a problem with the single sided junction approximation in this case. Ideally the C^{-2} -V relationship should be linear and extrapolation to the horizontal axis allows the diffusion voltage, V_D , to be determined, which is not possible in this case. It is postulated that interface states, non-uniform doping of the n-region or etching problems may be why the C-V data is non-linear.

By incorporating ZnSe or ZnS_xSe_{1-x} buffers, the PV characteristics of the “best” solar cells were generally lower than the CdS buffered cell. This was apart from an increase in short circuit current density the ZnSe cell which in turn increased the cell efficiency. By increasing the sulphur content, a general deterioration in PV performance was found. However, an increase in the high-energy spectral response with increased sulphur content was found. By increasing the “optical window” there is the potential for more photons to be pass through the buffer layer and be absorbed by the CdTe layer, thus contributing to solar generation.

The solar cells in this investigation were optimised with ZnSe buffer layers and using a deposition method (CSTE) that has not been reported. Therefore, three further points need to be considered:

1. Would the PV quality of these solar cells improve if all buffer layers across the range (of ZnS_xSe_{1-x} and CdS compounds) had been individually optimised?
2. What affect did the CdTe layers have on the buffers used? Use optimised CdTe layers (possible CSS deposited) to see if the quality of the absorber layer was detrimental to solar cell performance, not necessarily the buffer layers.
3. Would the use of a different absorber layer (possible $CuInSe_2$ or $CuInS_2$) produce better results?

Unfortunately these suggestions come under the title “Future Work”, as it was not possible to do these within the timescale of the current investigation.

To further investigate the potential of ZnS_xSe_{1-x} / CdTe solar cells, modelling of the devices was undertaken (section 8.4) and a breakdown of the energy band diagrams (section 8.5) has been discussed.

8.4 Modelling CdTe Based Devices

8.4.1 Characteristics of Modelled CdS / CdTe Solar Cells

To simulate the J-V and SR characteristics of CdTe based solar cells, the SCAPS software programme, developed by the University of Gent, was used [6]. This software allows the simulation of thin film heterojunction solar cells and permits different combinations of buffer and absorber materials. Supplied with the software is the data for a CdS / CdTe solar cell that was fabricated and used to test the accuracy of the simulation (see table 8.2). Therefore, this simulated CdS / CdTe cell was used first and the J-V characteristics are shown in figure 8.1. These data illustrate the effect on the PV characteristics of a cell under illumination with different buffer layer thickness. The increased buffer thickness reduces the short circuit current, as seen in table 8.1. A small increase in fill factor can be found but this is not large enough to increase the already reduced cell efficiencies. Also, the reduction in shunt resistance has little effect on the open circuit voltage.

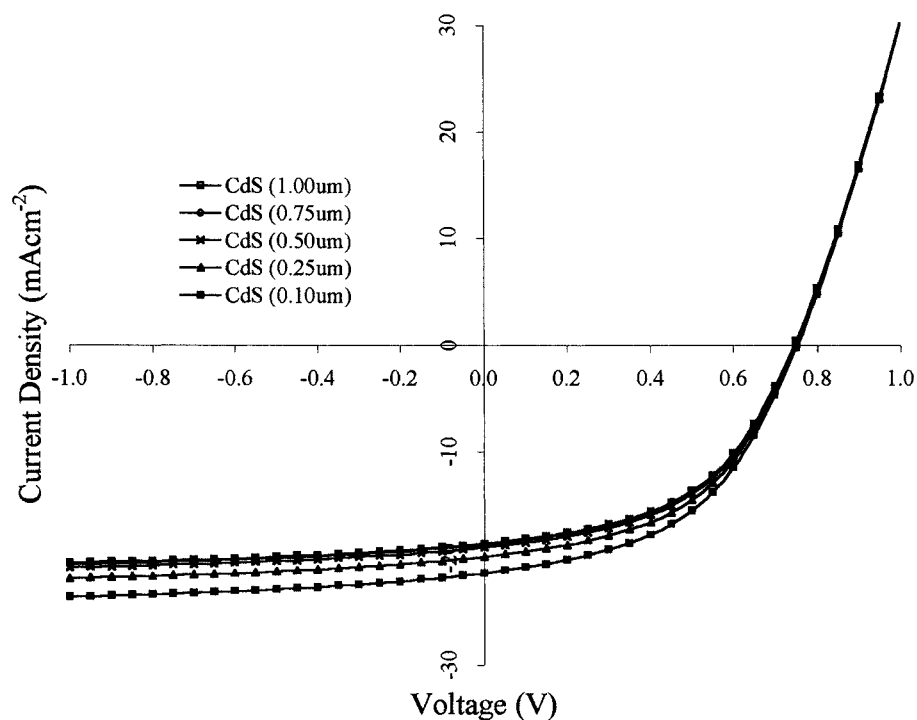


Figure 8.1. J-V Characteristics of CdS / CdTe Cells with Varying Buffer Thicknesses.

<i>CdS Thickness</i>	<i>V_{OC}</i>	<i>J_{SC}</i>	<i>FF</i>	<i>η</i>	<i>R_S</i>	<i>R_{SH}</i>
<i>(μm)</i>	<i>(mV)</i>	<i>(mAcm⁻²)</i>	<i>(%)</i>	<i>(%)</i>	<i>(Ω)</i>	<i>(Ω)</i>
0.10	753	21.36	48.2	7.7	7.9	463
0.25	749	19.83	48.8	7.2	8.2	515
0.50	746	18.96	49.1	7.0	8.3	551
0.75	745	18.69	49.3	6.9	8.4	562
1.00	745	18.59	49.3	6.8	8.4	566

Table 8.1. Characteristics of J-V Data for CdS / CdTe Cells.

The spectral response simulations of figure 8.2 illustrate the effect of the CdS thickness. At small thicknesses, the high energy photons can still contribute to the photo current. However, at large thicknesses, almost all these high energy photons are absorbed in the buffer layer

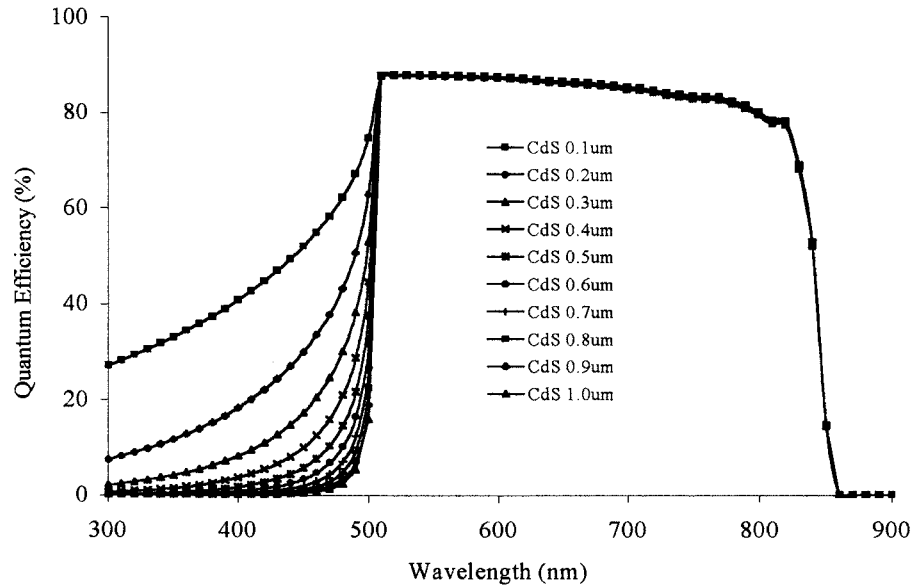


Figure 8.2. Quantum Efficiency versus Wavelength for CdS / CdTe Cells with Varying Buffer Thicknesses.

8.4.2 Characteristics of modelled $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe Solar Cells

To model the effects of zinc based buffers with CdTe absorber layers, additional parameter files were constructed and added to the database of materials within SCAPS. These parameters and that supplied with the program, are tabulated in 8.2. The values for ZnSe and ZnS were taken from the literature where appropriate. [7]. The $\text{ZnS}_{(0.50)}\text{Se}_{(0.50)}$ data was taken from the linear extrapolation of the two end binaries, apart from the energy bandgap, which allows for bowing (see figure 3.9). Also, the absorption data was in the form of a “lookup file”, the data of which was taken from [8]. The J-V data for the three zinc based buffers and CdTe absorbers are shown in figure 8.3 and table 8.3. When comparing this data and that of figure 8.1, for a CdS thickness of 0.1micron, the PV characteristics differ only slightly. The CdS cell has the highest V_{OC} , J_{SC} , FF and hence efficiency of the cells, where the ZnSe cell has the lowest.

		ZnSe	$\text{ZnS}_{0.50}\text{Se}_{0.50}$	ZnS	CdS*	CdTe*	CdTe(c)*
Thickness	(μm)	0.1	0.1	0.1	0.1	3.0	6.9
Bandgap	(eV)	2.67	3.00	3.6	2.42	1.5	1.5
Electron affinity	(eV)	4.1	4.0	3.9	4.5	4.3	4.3
Dielectric Permittivity (relative)		8.6	8.55	8.5	10	10	10
CB effective density of states	($\times 10^{18}\text{cm}^{-3}$)	1.5	1.5	1.5	1.5	1.3	1.3
VB effective density of states	($\times 10^{18}\text{cm}^{-3}$)	18	18	18	18	7.6	7.6
Electron thermal velocity	(cms^{-1})	10^7	10^7	10^7	10^7	10^7	10^7
Hole thermal velocity	(cms^{-1})	10^7	10^7	10^7	10^7	10^7	10^7
Electron mobility	(cm^2/Vs)	230	395	560	50	50	50
Hole mobility	(cm^2/Vs)	40	75	110	20	30	30
Shallow donor density	(cm^{-3})	10^{17}	10^{17}	10^{17}	10^{17}	0	0
Shallow acceptor density	(cm^{-3})	0	0	0	0	2×10^{14}	10^{13}
Number of additional defects		1	1	1	1	0	2

Table 8.2. Data Used in SCAPS Simulations of Thin Film Cells
(* Indicates Data Supplied with Program).

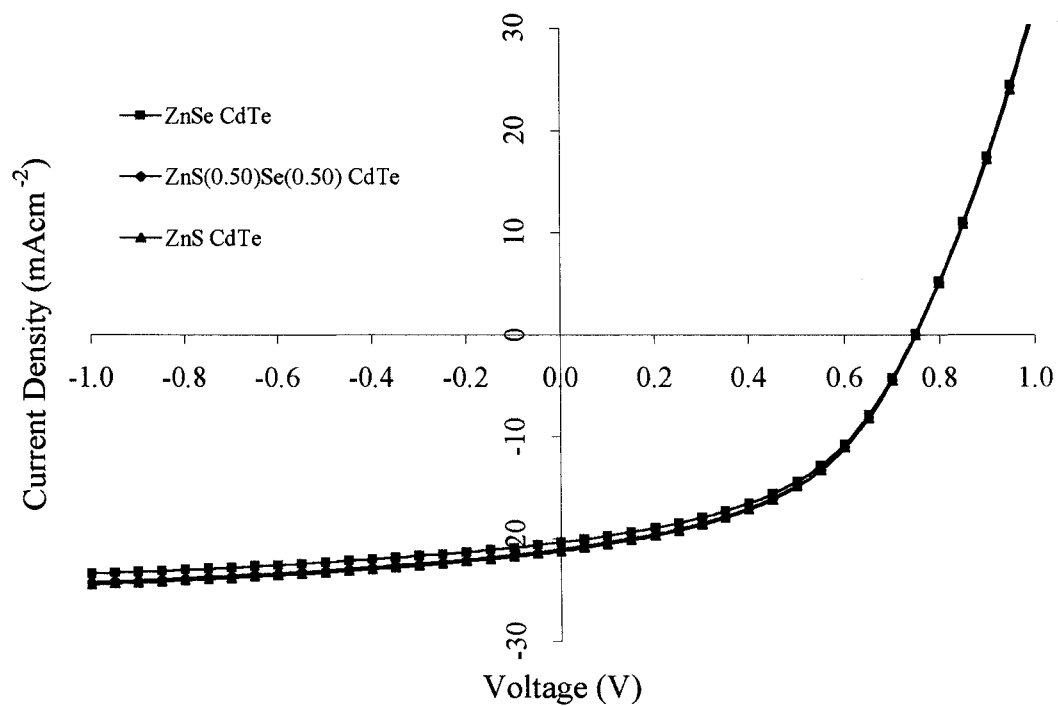


Figure 8.3. J-V Characteristics of ZnSe, ZnS_{0.50}Se_{0.50}, ZnS / CdTe Cells (buffers 0.1 μm thick).

<i>Window</i>	V_{OC}	J_{SC}	FF	η	R_S	R_{SH}
	(mV)	(mAcm ⁻²)	(%)	(%)	(Ω)	(Ω)
ZnSe	749	20.33	47.3	7.2	7.8	337
ZnS _{0.50} Se _{0.50}	750	21.00	47.0	7.4	7.5	321
ZnS	751	21.19	46.8	7.4	7.6	315

Table 8.3 Characteristics of J-V Data for ZnSe, ZnS_{0.50}Se_{0.50}, ZnS / CdTe Cells.

The spectral response data for the zinc cells are plotted in figure 8.4 and show the high energy bandedge moving to shorter wavelengths with increased sulphur content. This is the most likely reason as to why the ZnS then $\text{ZnS}_{0.50}\text{Se}_{0.50}$ have better PV characteristics than the ZnSe / CdTe cell. Since the simulation of figure 8.3 is with thin buffer layers (0.1micron) and high donor doping concentrations ($N_D=10^{17}\text{cm}^{-3}$), then by altering these parameters the cells can be further investigated. This was simulated in figure 8.5 and results tabulated in 8.4. The effects of $\text{ZnS}_{0.50}\text{Se}_{0.50}$ layer thickness on the J-V characteristics of a highly doped cell are minimal (ZnSSe 1.0 microns - high and ZnSSe 0.1 microns - high). However, by reducing the donor density to 10^{14}cm^{-3} , the effect of altering the layer thickness is clearly shown (ZnSSe 1.0 microns - low to ZnSSe 0.1microns - low).

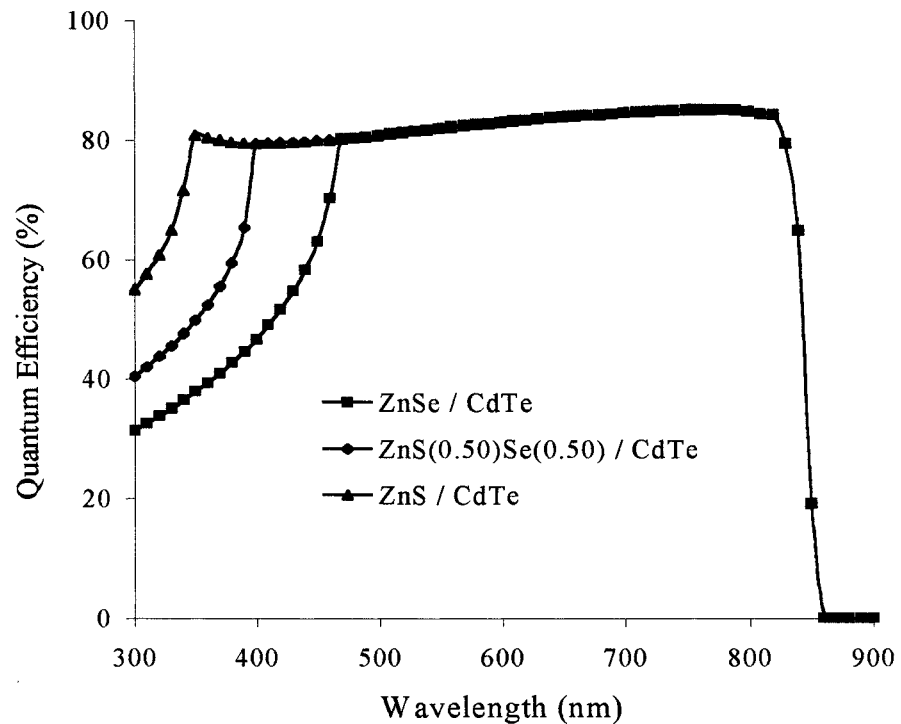


Figure 8.4. Quantum Efficiency versus Wavelength
for ZnSe, $\text{ZnS}_{0.50}\text{Se}_{0.50}$, ZnS / CdTe Cells.

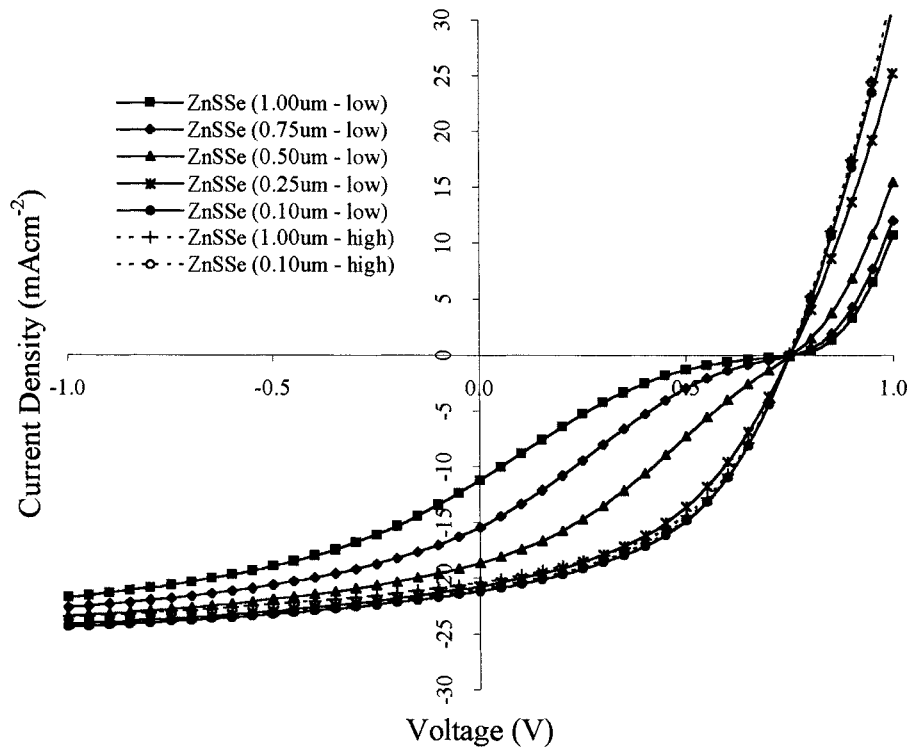


Figure 8.5. J-V Characteristics of $\text{ZnS}_{0.50}\text{Se}_{0.50}$ / CdTe Cells with Varying Donor Densities and Buffer Thicknesses.

$\text{ZnS}_{0.50}\text{Se}_{0.50}$ Thickness	Donor Density		V_{oc}	J_{sc}	FF	η
(μm)		(cm^{-3})	(mV)	(mAcm^{-2})	(%)	(%)
1.00	low	10^{14}	761	11.25	15.6	1.3
0.75	low	10^{14}	758	15.43	20.6	2.4
0.50	low	10^{14}	754	18.64	30.3	4.3
0.25	low	10^{14}	751	20.75	43.7	6.8
0.10	low	10^{14}	751	21.18	46.7	7.4
1.00	high	10^{17}	749	20.40	47.2	7.2
0.10	high	10^{17}	750	21.00	47.0	7.4

Table 8.4. Characteristics of J-V Data for $\text{ZnS}_{0.5}\text{Se}_{0.5}$ / CdTe Cells.

8.5 Formation of the Energy Band Diagrams

As previously discussed in Chapter 2, the Anderson model assumes that each semiconductor is characterised by its energy bandgap, electron affinity and work function. This model also maintains that the semiconductor interface should be an abrupt heterojunction. To construct an energy band diagram of CdS or $\text{ZnS}_x\text{Se}_{1-x}$ n-type region and p-CdTe, an initial approach is to use this model. The two factors that can be considered constant for the individual semiconductors are their energy bandgap, E_g , and electron affinity, χ . The work function however, is dependent upon the level of doping and for an n-type semiconductor as shown in chapter 2

$$\phi_n = \chi_n + \delta_n \quad 8.1.$$

and

$$\delta_n = \left(\frac{-kT}{e} \right) \ln \left(\frac{N_D}{N_C} \right) \quad 8.2.$$

It has been shown that N_C can be given by [9]

$$N_C = 2.5 \times 10^{19} (m_n)^{3/2} \left(\frac{T}{300} \right) \quad 8.3.$$

where m_n is the effective mass. Conversely, for a p-type semiconductor, the work function is given by

$$\phi_p = \chi_p + E_g - \delta_p \quad 8.4.$$

and

$$\delta_p = \left(\frac{-kT}{e} \right) \ln \left(\frac{N_A}{N_V} \right) \quad 8.5.$$

N_V can be written as [9]

$$N_V = 2.5 \times 10^{19} (m_p)^{3/2} \left(\frac{T}{300} \right) \quad 8.6.$$

Figure 8.6 shows the energy band diagram constructed using this model. The discontinuity in the conduction bandedge (ΔE_c) is equal to the difference in electron affinities and is given by

$$\Delta E_c = \chi_p - \chi_n \quad 8.7.$$

and for the valance band the discontinuity ΔE_v can be written as

$$\Delta E_v = (E_{g_n} - E_{g_p}) - (\chi_p - \chi_n) \quad 8.8.$$

The final characteristic of the energy band diagram of figure 8.6 is the built-in voltage (V_D) and is due to the difference in work functions.

$$\begin{aligned} V_D &= \phi_p - \phi_n \\ V_D &= (\chi_p + E_{g_p} - \delta_p) - (\chi_n + \delta_n) \end{aligned} \quad 8.9.$$

In order to estimate the built-in voltage for a CdS / CdTe junction, the energy separations δ_n and δ_p must be calculated. However, both of these parameters, like the work functions, (ϕ_p and ϕ_n) are dependent upon the respective doping levels of the semiconductor. Therefore, the built-in voltage must be estimated from sample data. Table 8.5 shows the data used to determine the model characteristics, and where necessary, data was obtained from the literature [7] and the modelled data (SCAPS 2.3.) from section 8.4.

Cell details	n-buffer						p-CdTe								
	E _{g_n}	χ _n	m _n	N _D	N _C	δ _n	E _{g_p}	χ _p	m _p	N _A	N _V	δ _p	ΔE _c	ΔE _v	V _D
	(eV)	(eV)		(cm ⁻³)	(cm ⁻³)	(eV)	(eV)	(eV)		(cm ⁻³)	(cm ⁻³)	(eV)	(eV)	(eV)	(V)
SCAPS 2.3	2.42	4.50	0.21	10 ¹⁷	1.50×10 ¹⁸	0.070	1.50	4.28	0.37	2×10 ¹⁴	7.60×10 ¹⁸	0.273	0.22	0.70	0.94
This work															
CdS/CdTe	2.42	4.50	0.21	*10 ¹⁷	2.41×10 ¹⁸	0.082	1.50	4.28	0.37	8.1×10 ¹³	5.63×10 ¹⁸	0.288	0.22	0.70	0.91
ZnSe/CdTe	2.67	4.09	0.15	*10 ¹⁷	1.45×10 ¹⁸	0.069	1.50	4.28	0.37	2.8×10 ¹³	5.63×10 ¹⁸	0.316	0.19	0.98	1.31
ZnS _{0.50} Se _{0.50} /CdTe	2.98	4.00	0.20	*10 ¹⁷	2.24×10 ¹⁸	0.080	1.50	4.28	0.37	2.0×10 ¹³	5.63×10 ¹⁸	0.324	0.28	1.20	1.38
ZnS/CdTe	3.60	3.90	0.25	*10 ¹⁷	3.13×10 ¹⁸	0.089	1.50	4.28	0.37	3.8×10 ¹⁴	5.63×10 ¹⁸	0.248	0.38	1.72	1.54

Table 8.5. Table Showing Calculated Built-in Potentials for n-Buffer Layer / p-CdTe Heterojunctions
 (* Estimated Considering Single Sided Junction Theory)

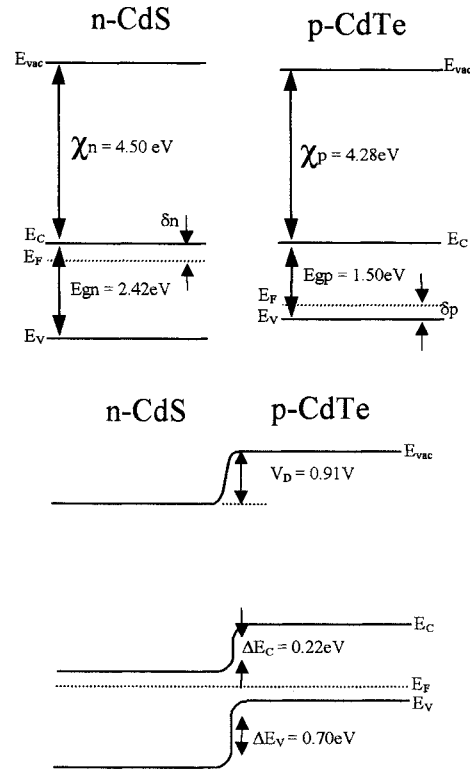


Figure 8.6. Energy Band Diagram for n-CdS / p-CdTe Heterojunction

Using the Anderson model, the energy band diagrams for n-ZnSe and n-ZnS with a p-CdTe heterojunction partner have been produced, see figure 8.7. Since the electron affinity of n-ZnSe and n-ZnS (and hence n-ZnS_xSe_{1-x}) is less than that of p-CdTe, a conduction band spike is produced. It can also be seen that the valance band discontinuity is increased for n-ZnSe, when compared to the n-CdS, and is much larger for n-ZnS. Finally, the energy band diagram for n-ZnS_{0.50}Se_{0.50} is produced in figure 8.8. The value for E_g was taken from the energy bandgap versus alloy composition data for n-ZnSSe of figure 3.9 and allows for system bowing. The values for electron affinity and effective mass assume a linear response between the two end binaries (i.e. ZnSe and ZnS).

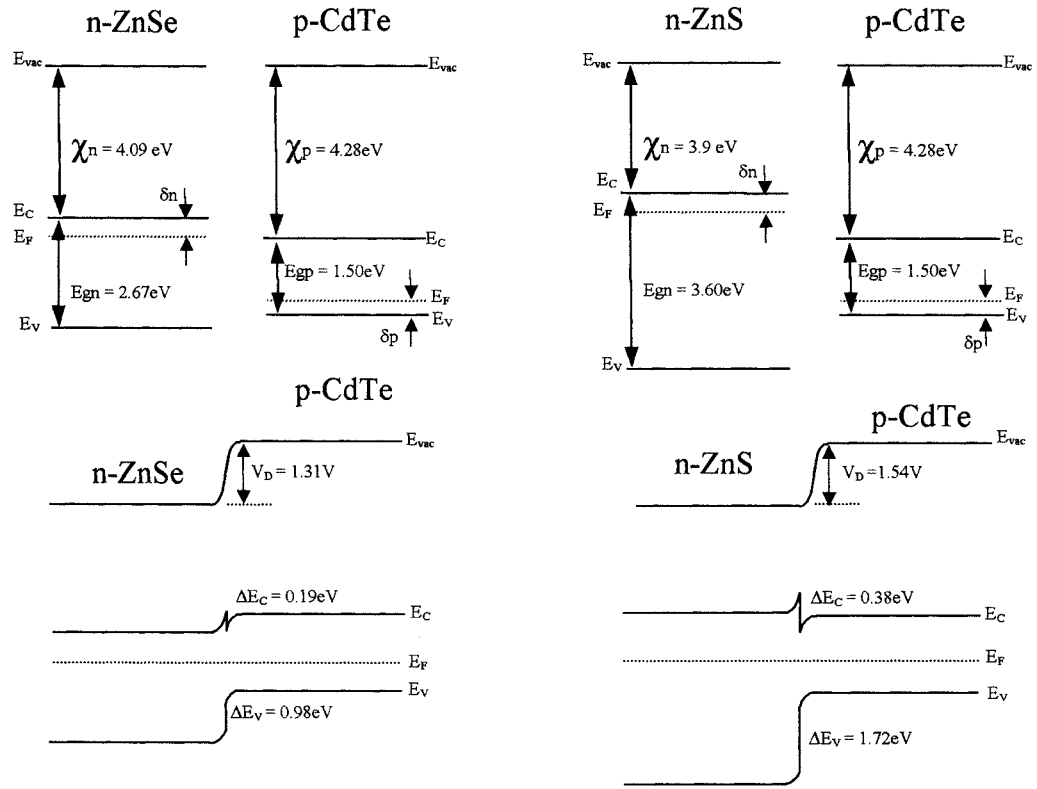


Figure 8.7. Energy Band Diagrams for n-ZnSe / p-CdTe and n-ZnS / p-CdTe Heterojunctions

As shown, the Anderson model predicts discontinuities in the bandedge, which are dependent upon the energy bandgaps and electron affinities of the semiconductor materials. The discontinuity in the conduction band (ΔE_C) can affect the heterojunction's (and hence the solar cell's) performance. When $\Delta E_C < 0$ (i.e. no conduction band spike) as shown in figure 8.6, then the built-in voltage is reduced, which in turn decreases the open circuit voltage. On the other hand, when $\Delta E_C > 0$, (i.e. a conduction band spike is formed) as shown in figures 8.7 and 8.8, a change in the transport mechanisms across the junction can occur [10].

A second factor relating to the Anderson model is the question of abruptness. Many thin film heterojunctions are fabricated at high temperatures where interdiffusion of the p and n-type material almost certainly occurs. Fahrenbruch and Bube [10] discussed this effect with reference to other workers, concluding that a graded junction could be formed that would potentially smear out or lower the conduction band spike to such an extent that the carrier flow was unimpeded.

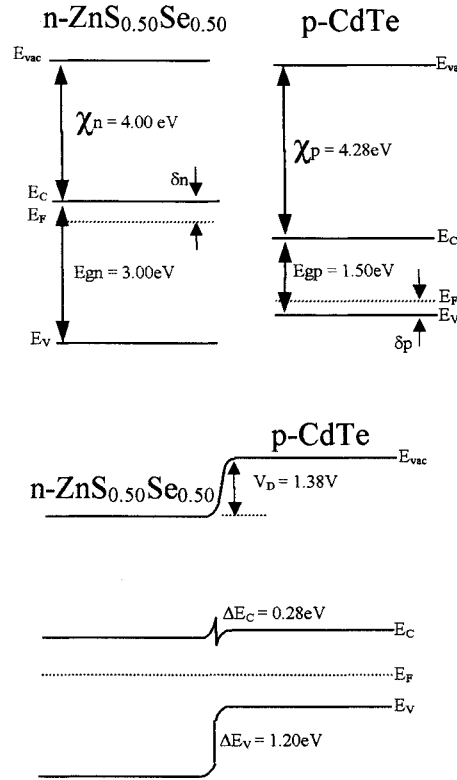


Figure 8.8. Energy Band Diagram for n-ZnS_{0.50}Se_{0.50} / p-CdTe Heterojunction

Finally, the lack of consideration of interface states and dipoles of this model needs to be addressed. Interface states arise from the properties of the lattice constant or the process of fabrication of the heterojunction. When an appreciable lattice mismatch occurs, the chances of unpaired valance band electrons, or dangling bonds, greatly increase. The question is whether these interface states are electrically active or passive. If electrically active, the interface states can affect the heterojunction properties in two ways, (i) any charge stored at the interface states can introduce further distortion of the band profile at the junction interface. (ii) high density of interface states can become recombination sites that increase the reverse saturation current density J_0 .

A large density of surface states and Fermi level pinning form interfacial dipoles. At the interface, these two factors allow the formation of a near metallic layer at the surface, therefore during fabrication of the heterojunction, these metallic layers form a dipole. As with interface states, dipoles can produce additional band bending at the interface.

8.6 References

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Chapter Nine

Conclusions

9.0 Conclusions

The aim of this work was to grow and characterise ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers to determine if they were suitable materials for use in thin film solar cells. Successful deposition of ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers was performed using close-spaced thermal evaporation (CSTE). This low cost deposition technique has good potential to be scaled up for commercial applications. CSTE has produced coatings in which a systematic growth in grain size with increasing substrate temperature was found. By altering the source temperature, substrate temperature and source – substrate distance, the morphology of the thin films could be controlled. SEM investigations found that pinhole free layers could be grown with the use of a tantalum baffle. In the case of $\text{ZnS}_x\text{Se}_{1-x}$ layers, the grain size was shown to increase with increasing sulphur content, confirmed by both SEM and AFM investigations. In addition, successful deposition of pinhole free $\text{ZnS}_x\text{Se}_{1-x}$ films was performed.

The structure of ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ was further investigated using the X-ray diffraction data. These data show there is a tendency for ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ to form with a sphalerite structure, with a preferred orientation about the (111) peak. The assumption was made that $\text{ZnS}_x\text{Se}_{1-x}$ obeys Vegards law, which enabled the alloy composition to be determined from the linear relationship between the end binaries. An observed colour variation between orange and milky white was found with the as-deposited $\text{ZnS}_x\text{Se}_{1-x}$ coatings, which could lead to commercial applications in scalable optical filters in the UV to visible region.

Optical data show steep absorption edges and good transmittance in the pass region of the ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ layers. The energy bandgap data of ZnSe indicated a relationship with the substrate temperature, with a preference of 200 to 300°C. A systematic shift in energy bandgap with $\text{ZnS}_x\text{Se}_{1-x}$ alloy composition was found, indicating excellent mixing of the sulphur and selenium anions to produce homogeneous alloys, supported by the XRD data in which only a single phase material was observed. The energy bandgap of this ternary alloy system was also found to have a non-linear relationship between the end binaries, which could be fitted using a quadratic equation. An optical bowing parameter of $0.51 \pm 0.05 \text{ eV}$ was determined, which is in good agreement with other workers (see section 3.3). Thin layers of $\text{ZnS}_x\text{Se}_{1-x}$ deposited on SnO_2 coated glass substrates enabled the series

resistance through the layers to be reduced to less than $60\Omega\text{cm}^{-2}$ (allowing for contact area).

From the literature it was found that preparation by different growth / deposition methods has indicated that $\text{ZnS}_x\text{Se}_{1-x}$ is produced commonly with the sphalerite structure. However, high sulphur content in some cases produces a wurtzite composition, which was not found in this work. The tuneability of $\text{ZnS}_x\text{Se}_{1-x}$, again confirmed in this work, agrees with other investigations, which would allow application in lattice-matching of $\text{ZnS}_x\text{Se}_{1-x}$ with semiconductor substrates such as GaAs, GaP and Si. The optical properties of $\text{ZnS}_x\text{Se}_{1-x}$ appear to be the material's most agreeable quality and the ability to operate in the blue-UV end of the spectrum could extend the range of optoelectronic device applications.

Since the inception of this work, other material data has been published on $\text{ZnS}_x\text{Se}_{1-x}$. Gordillo et. al. [1] (2004) produced $\text{ZnS}_x\text{Se}_{1-x}$ by co-evaporation of ZnSe and ZnS. This work shows a linear relationship between the end binaries, systematic shift in energy bandgap with alloy composition, optical bowing (bowing parameter not calculated) and a cubic polycrystalline structure. All of their results are in agreement with the work discussed here, and previously published in 2002 [2].

To partner the ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ buffer layers in a thin film heterojunction, CdTe absorber layers were grown. From the outset it was intended that the CdTe should be deposited in the same vacuum chamber as the buffer layers. This was to reduce the risk of interfacial contamination, but in addition, since CSTE has the potential to be used in commercial applications, it would be more cost effective if the same deposition plant were used.

Successful deposition of CdTe layers was achieved, and the optimum substrate temperature of the as-deposited coatings was found to be 350°C , with a source temperature of 600°C . The morphology of the as-deposited CdTe, was found to have small grains, which would indicate that CSTE in this case produces films closer to that observed with thermal evaporation than CSS. However, a growth rate of $1.6\mu\text{m}\cdot\text{min}^{-1}$ would suggest that the process is closer to close-spaced sublimation. This would therefore indicate that CSTE is somewhere between vacuum evaporation and CSS in terms of film production and operation. The diffraction data of the lower substrate temperature as-deposited CdTe show mixed phases, which by introducing higher substrate temperatures, the cubic phase prevailed.

The post deposition CdCl_2 treatment, which is an essential processing step when fabricating CdTe based solar cells, produced grain growth in the CdTe layers, which was confirmed by both SEM (and histograms) and XRD data using the Scherrer technique. The texture coefficient of the as-deposited CdTe (higher temperatures) indicated cubic phases with a preferred orientation of the (111) peak, and after the CdCl_2 treatment, the layers become more random. The CdCl_2 treatment facilitated optical measurements of the CdTe layers, of which an energy bandgap of 1.5eV was determined. This post deposition heat treatment also produced p-type conversion and therefore a reduction in resistivity.

When reviewing the literature, the critical issue concerning CdTe thin film devices is the multiple processing steps such as the CdCl_2 treatment, pre and post-deposition annealing that are necessary to produce high efficiency cells. Solar cells in this work were fabricated in the superstrate configuration: glass / SnO_2 / buffer / CdTe / back contact. The characteristics of the untreated cells show how the lack of buffer layer doping and the lack of p-type absorber layer conversion adversely affect the photovoltaic properties. By introducing the post deposition CdCl_2 treatment, the current – voltage characteristics of the cells were improved, giving short circuit current densities approaching 5mAcm^{-2} . Optimisation of the buffer layers was undertaken (in chapter 5), the success of which was determined when fabricated in cells with CdTe. By using thinner buffer layers it was found that the PV properties of the cells could be improved. Optimisation of the deposition properties culminated in “best solar cells” produced in this work, fabricated with the following critical steps:

- (i) $\text{ZnS}_x\text{Se}_{1-x}$ buffer layers, substrate – source distance 11mm, T_{sub} 200°C, T_{source} 600°C and thickness $\sim 0.6\mu\text{m}$.
- (ii) CdTe absorber layers substrate – source distance 11mm, T_{sub} 350°C, T_{source} 600°C and thickness $> 5\mu\text{m}$.
- (iii) CdCl_2 dip in 50% solution for 1 minute, followed by air anneal at 440°C for 20 minutes.

ZnSe / CdTe solar cells were fabricated with the best cell producing PV characteristics of: short circuit current density 17mAcm^{-2} , open circuit voltage 460mV and efficiency approaching 3%. This cell also had a diode factor of 1.6 and reverse saturation current density, $1.7 \times 10^{-7}\text{mAcm}^{-2}$, approaching that obtained with CdS / CdTe devices. The spectral response of this cell indicated a higher contribution from high energy photons than low energy photons above the CdTe bandedge.

$\text{ZnS}_x\text{Se}_{1-x}$ / CdTe cells were also successfully fabricated. These devices demonstrated a systematic reduction in photovoltaic characteristics with increasing alloy composition. This indicates that an increase in sulphur, for devices fabricated in this manner, may not be beneficial to device performance.

The spectral response of all ZnSe and $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe devices demonstrated a systematic shift to shorter wavelengths with increasing alloy composition. This was a desire of this work in an attempt to increase the contribution of the blue response of the cell, therefore increasing the photocurrent and hence efficiency. The position of the junction also showed signs of movement towards the long wavelength edge with increasing sulphur content, indicating that buffer layers containing sulphur may show a tendency to produce buried junctions.

Problems were encountered with the capacitance – voltage measurements and it is postulated that this could be due to (i) application of the single sided junction approximation, (ii) inferior buffer doping or (iii) excessive etching before back contact deposition.

Modelling of the heterojunction properties was performed. These data show an increase in PV characteristics with thinner layers. Also, the shift to shorter wavelengths with increasing alloy composition confirmed the experimental data. Models also show that the buffer layer must be highly doped to achieve high efficiency solar cells.

Using data from the literature and experimental results obtained in this work, the energy band profile of $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe heterojunctions was determined using the Anderson method. These data illustrate an increase in valence and conduction band barriers between the $\text{ZnS}_x\text{Se}_{1-x}$ and CdTe with increasing alloy composition. These barrier discontinuities and a lattice mismatch could cause problems with $\text{ZnS}_x\text{Se}_{1-x}$ / CdTe junctions, however, if a graded or buried junction is formed by control of the fabrication parameters, then for thin film solar cells this may not necessarily be a problem.

The future of $\text{ZnS}_x\text{Se}_{1-x}$ may not necessarily be in a heterojunction partnership with CdTe. As discussed in chapter 3, $\text{ZnS}_x\text{Se}_{1-x}$ can be lattice matched with other compounds. Other workers have also produced $\text{ZnS}_x\text{Se}_{1-x}$ buffered solar cells (deposited using other methods) and combined with alternative absorber layers to produce: $\text{ZnS}_x\text{Se}_{1-x} / \text{CuInS}_2$ [3], $\text{ZnS}_x\text{Se}_{1-x} / \text{CIGSS}$ [4].

The unknown factor with CdTe could be with the environmental issues. The impending European RoHS directive [5] does not apply to PV at present. However, if this were the case then a concentration of 0.01% per homogeneous element would stop the use of CdTe in PV completely.

9.1 References

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- [2] S. Armstrong, P.K. Datta, R.W. Miles, "Properties of Zinc Sulphur Selenide Deposited using a Close-Spaced Sublimation Method", Thin Solid Films 403-404 (2002), pages 126 to 129.
- [3] K.T.R. Reddy, Y.P.V. Subbaiah, T.B.S. Reddy, R.W. Miles, "Investigations on $\text{CuInS}_2 / \text{ZnS}_{0.5}\text{Se}_{0.5} / \text{ZnO}$ Thin Film Solar Cells", Technical Digest of the International PVSEC – 14, (2004), pages 699 to 700.
- [4] A. Ennaoui, S. Siebentritt, M.Ch. Lux-Steiner, R. Riedl, F. Karg, "High-Efficiency Cd-Free CIGSS Thin Film Solar Cells with Solution Grown Zinc Compound Buffer Layers", Solar Energy Materials and Solar Cells 67, (2001), pages 31 to 40.
- [5] Restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), European Community Directive 2002/95/EC

Appendix A – List of Symbols

Symbol	Definition	Dimensions
a	Lattice constant	\AA
A	Homojunction Ideality (perfection) factor	
A_o	Cross sectional area	cm^2
C	Capacitance	F
C	Capacitance per unit area	Fcm^{-2}
D	Diffusion coefficient	$\text{cm}^2\text{sec}^{-1}$
D_n	Diffusion coefficient for electrons	$\text{cm}^2\text{sec}^{-1}$
D_p	Diffusion coefficient for holes	$\text{cm}^2\text{sec}^{-1}$
e	Magnitude of electronic charge	C
E	Energy	eV
E_A	Acceptor level energy	eV
E_C	Bottom of conduction band	eV
E_D	Donor level energy	eV
E_F	Fermi level energy	eV
E_g	Energy bandgap	eV
E_V	Top of valence band	eV
\mathcal{E}_m	Electric Field	Vcm^{-1}
FF	Fill factor	%
G	Carrier generation rate	$\text{cm}^{-3}\text{sec}^{-1}$
h	Planck's constant	Js
\hbar	Planck's constant ($\hbar = h/2\pi$)	Js
$h\nu$	Photon energy	eV
I	Current	A
I_L	Light generated current	A
I_{mp}	Current at maximum power point	A
I_o	Reverse saturation current	A
I_{oo}	Pre-exponential factor of I_o	A
I_{SC}	Short circuit current	A
J	Current density	Acm^{-2}
J_o	Reverse saturation current density	Acm^{-2}
J_{oo}	Pre-exponential factor of J_o	Acm^{-2}
J_{SC}	Short circuit current density	Acm^{-2}
k	Boltzmann constant	JK^{-1}
kT	Thermal energy	eV
L_a	Absorption length	cm
L	Minority carrier diffusion length	cm
L_n	Minority carrier diffusion length for electrons	cm
L_p	Minority carrier diffusion length for holes	cm
m	Effective mass	kg
m_n, m_p	Effective mass, semiconductor	kg
n	Heterojunction Ideality (perfection) factor	
n	Electron concentration	cm^{-3}
n_n	Electron concentration in n-type material	cm^{-3}
n_p	Electron concentration in p-type material	cm^{-3}
n_i	Intrinsic carrier density	cm^{-3}
N	Doping concentration	cm^{-3}
N_A	Acceptor impurity density	cm^{-3}

N_C	Effective density of states in conduction band	cm^{-3}
N_D	Donor impurity density	cm^{-3}
N_V	Effective density of states in valence band	cm^{-3}
p	Hole concentration	cm^{-3}
p_n	Hole concentration in n-type material	cm^{-3}
p_p	Hole concentration in p-type material	cm^{-3}
P_{in}	Input power per unit area	Wcm^{-2}
P_m	Power at maximum power point	W
R	Resistance	Ω
$R_P (R_{SH})$	Parallel resistance	Ω
R_S	Series resistance	Ω
V	Voltage	V
V_D	Diffusion or Built in voltage	V
V_{mp}	Voltage at maximum power point	V
V_{oc}	Open circuit voltage	V
W	Depletion layer width	cm
α	Optical absorption coefficient	cm^{-1}
δ_n, δ_p	Fermi level displacement	eV
ϵ_r	Dielectric constant ($\epsilon_r = \epsilon_s / \epsilon_o$)	
ϵ_s	Permittivity of semiconductor	Fcm^{-1}
ϵ_o	Permittivity of free space	Fcm^{-1}
η	Solar power conversion efficiency	$\%$
μ_n	Electron mobility	$\text{cm}^2 \text{V}^{-1} \text{sec}^{-1}$
μ_p	Hole mobility	$\text{cm}^2 \text{V}^{-1} \text{sec}^{-1}$
ρ_s	Sheet resistance	$\Omega.\square^{-1}$
ρ_s	Resistivity	$\Omega.\text{cm}$
τ	Minority carrier lifetime	s
τ_n	Minority carrier lifetime, electrons	s
τ_p	Minority carrier lifetime, holes	s
ϕ	Work function	V
ϕ_m	Work function, metal	V
ϕ_n, ϕ_p	Work function, semiconductor	V
χ	Electron affinity	eV

Appendix B – List of Publications

S. Armstrong, P. K. Datta, R. W. Miles, “Properties of Zinc Sulphur Selenide Deposited using a Close-Spaced Sublimation Method”, Thin Solid Films 403-404 (2002), pages 126 to 129.

S. Armstrong, P. K. Datta, R. W. Miles, “Thermal Evaporation of $\text{ZnS}_x\text{Se}_{1-x}$ for Application in Thin Film Solar Cells”, 17th European Photovoltaics Specialists Conference, Munich, 2001.